MODEL NAME : *CKF50/CKA50*

PCB NO : *LA-E992P*

BOM P/N :

451A7631L51
451A7631L52
451A7631L01
451A7631L02

Dell/Compal Confidential

Schematic Document

KABYLAKE-H
N17E

Firestar/Armani

2017-07-25

Rev: 1.0 (A00)

Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2011/08/25

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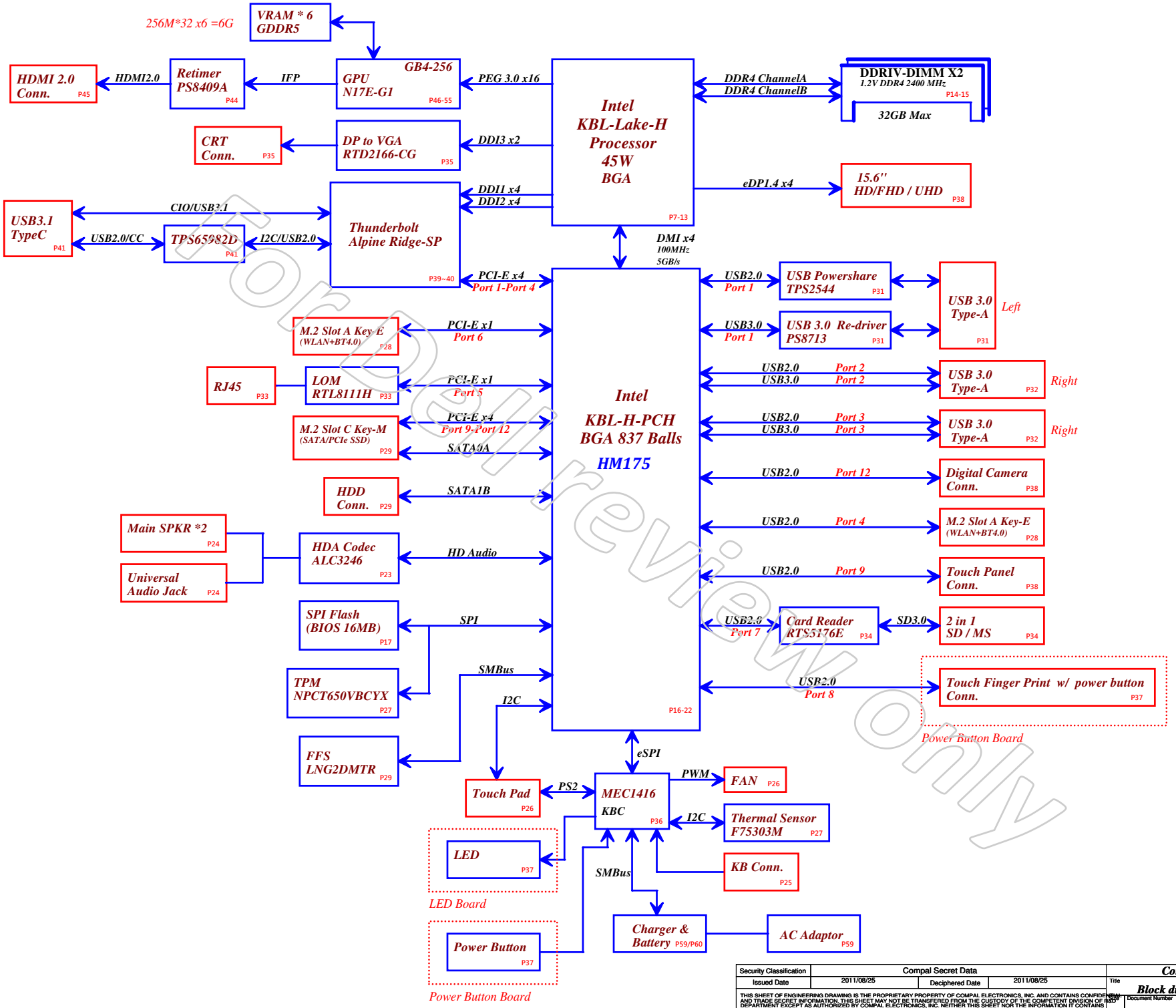
Title: *Cover Page*

Size: | Document Number: *LA-E992P* | Rev: 1.0(A00)

Date: Tuesday, July 25, 2017 | Sheet 1 of 77



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Issued Date	2011/08/25	Deciphered Date 2011/08/25	Title: Block diagram
Document Number	LA-E992P		Rev 1.0(A00)
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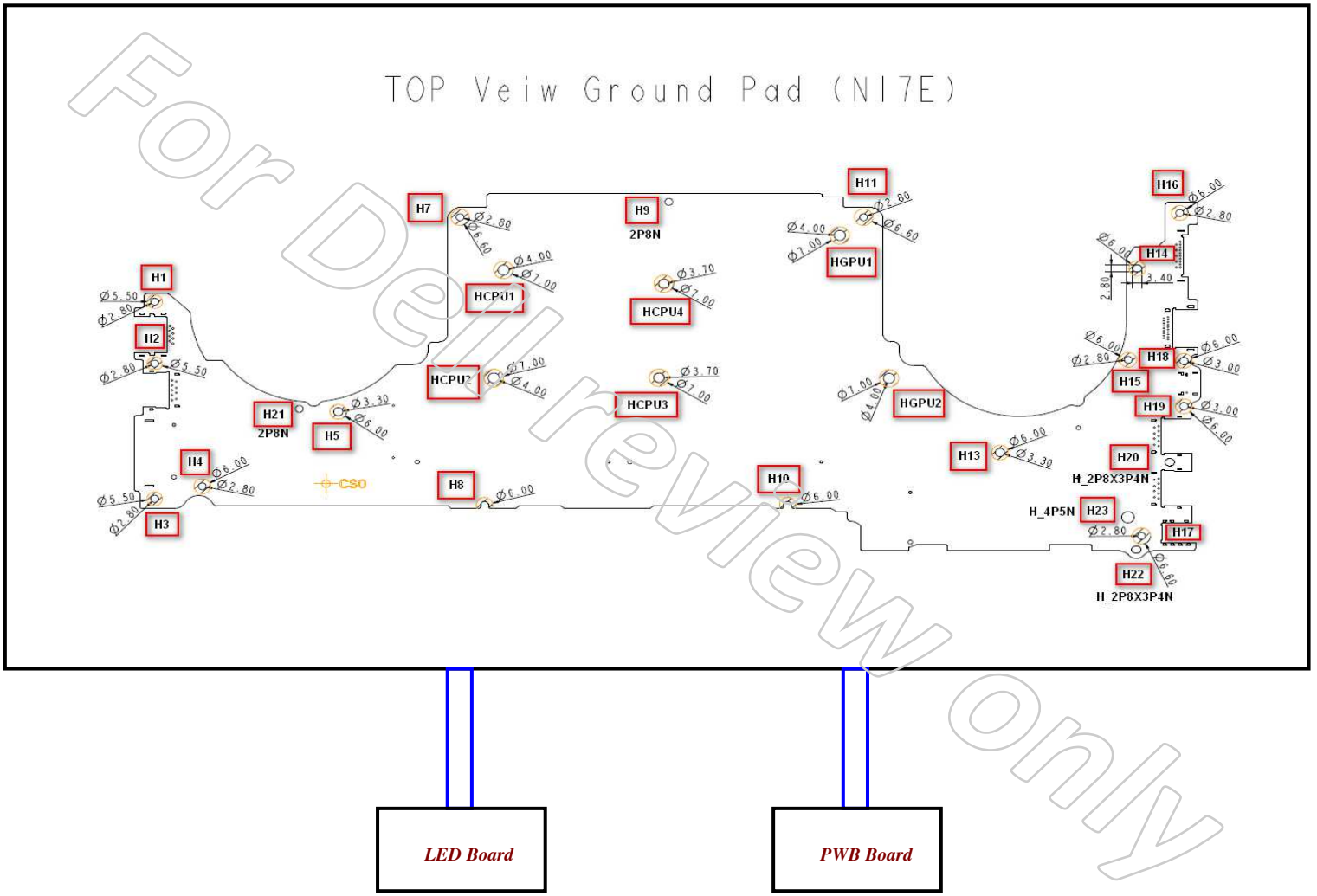
Project Code :
File Name :

ME Hole Location
Base on ME 0505

M/B



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Title: DB block diagram			
Size	Document Number: LA-E992P		Rev: 1.0(A00)
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Refer Page 36

PCI EXPRESS	DESTINATION	USB3	DESTINATION
Lane 1	Alpine Ridge - SP	7	None
Lane 2		8	None
Lane 3		9	None
Lane 4		10	None
Lane 5	LOM		
Lane 6	NGFF - WLAN + BT		
Lane 7	None		
Lane 8	None	SATA	DESTINATION
Lane 9	NGFF - SSD	0A	NGFF - SSD
Lane 10		1A	None
Lane 11			
Lane 12			
Lane 13	None	0B	None
Lane 14	None	1B	HDD
Lane 15	None	2	None
Lane 16	None	3	None

CLK_PCIE	DESTINATION	CLK_REQ	DESTINATION
0	None	0	None
1	None	1	None
2	LOM	2	LOM
3	NGFF - WLAN + BT	3	NGFF - WLAN + BT
4	None	4	None
5	Alpine Ridge - SP	5	Alpine Ridge - SP
6	NGFF - SSD	6	NGFF - SSD
7	GPU	7	GPU
8	None	8	None
9	None	9	None
10	None	10	None
11	None	11	None
12	None	12	None
13	None	13	None
14	None	14	None
15	None	15	None

USB2	DESTINATION
1	USB JUSB3 (Left Side)
2	USB JUSB1 (Right Side)
3	USB JUSB2 (Right Side)
4	NGFF - WLAN + BT
5	None
6	None
7	CARD READER
8	Finger Print
9	Touch screen
10	None
11	None
12	CAMERA

Symbol Note :

: means Digital Ground

: means Analog Ground

USB3	DESTINATION
1	USB JUSB3 (Left Side)
2	USB JUSB1 (Right Side)
3	USB JUSB2 (Right Side)
4	None
5	None
6	None

DDI	DESTINATION
1	Alpine Ridge
2	Alpine Ridge
3	DP to VGA

Board ID	Resistor
X00	10K
X01	17.8K
X02	27K
X03	37.4K
A00	49.9K

Table 1-3. PCH-H HSIO Detail (Lane 1-14)

SKU	1	2	3	4	5	6	7	8	9	10	11	12	13	14
H110	USB 3.0/ OTG	USB 3.0	USB 3.0	USB 3.0	N/A	N/A	N/A	N/A	N/A	LAN Only	PCIe/ LAN	PCIe	PCIe	PCIe
H170	USB 3.0/ OTG	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	PCIe	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe	PCIe
HM170/ HM175	USB 3.0/ OTG	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0/ PCIe	USB 3.0/ PCIe	PCIe	PCIe / LAN	PCIe/ LAN	PCIe	PCIe	PCIe
QM170/ QM175	USB 3.0/ OTG	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0/ PCIe	USB 3.0/ PCIe	PCIe	PCIe / LAN	PCIe/ LAN	PCIe	PCIe	PCIe
Z170	USB 3.0/ OTG	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0/ PCIe	USB 3.0/ PCIe	USB 3.0/ PCIe	USB 3.0/ PCIe/LAN	PCIe/ LAN	PCIe	PCIe	PCIe
B150	USB 3.0/ OTG	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	N/A	N/A	N/A	LAN Only	PCIe/ LAN	PCIe	PCIe	PCIe
Q150	USB 3.0/ OTG	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	N/A	LAN Only	PCIe/ LAN	PCIe	PCIe	PCIe
Q170	USB 3.0/ OTG	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0/ PCIe	USB 3.0/ PCIe	USB 3.0/ PCIe	USB 3.0/ PCIe/LAN	PCIe / LAN	PCIe	PCIe	PCIe

Table 1-4. PCH-H HSIO Detail (Lane 15-26) (Sheet 1 of 2)

SKU	15[1]	16[1]	17	18	19[1]	20[1]	21	22	23	24	25	26
H110	PCIe/ LAN	PCIe	N/A	LAN Only	SATA0/ LAN	SATA1	SATA	SATA	N/A	N/A	N/A	N/A
H170	PCIe/LAN /SATA0	PCIe/ SATA1	PCIe	PCIe/ LAN	PCIe/LAN / SATA0	PCIe/ SATA1	PCIe/ SATA	PCIe/ SATA	SATA	SATA	PCIe	PCIe
HM170/ HM175	PCIe/LAN /SATA0	PCIe/LAN/ SATA1	PCIe	PCIe/ LAN	PCIe/LAN/ SATA0	PCIe/ SATA1	PCIe/ SATA	PCIe/ SATA	N/A	N/A	N/A	N/A
QM170/ QM175	PCIe/LAN /SATA0	PCIe/LAN/ SATA1	PCIe	PCIe/ LAN	PCIe/ LAN/ SATA0	PCIe/ SATA1	PCIe/ SATA	PCIe/ SATA	N/A	N/A	N/A	N/A
Z170	PCIe/LAN /SATA0	PCIe/ SATA1	PCIe	PCIe/ LAN	PCIe/LAN / SATA0	PCIe/ SATA1	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe	PCIe
B150	PCIe/LAN /SATA0	PCIe/ SATA1	PCIe	PCIe/ LAN	SATA0	SATA1	SATA	SATA	SATA	SATA	N/A	N/A
Q150	PCIe/LAN /SATA0	PCIe/ SATA1	PCIe	PCIe/ LAN	PCIe/LAN / SATA0	PCIe/ SATA1	SATA	SATA	SATA	SATA	N/A	N/A
Q170	PCIe/LAN /SATA0	PCIe/ SATA1	PCIe	PCIe/ LAN	PCIe/LAN / SATA0	PCIe/ SATA1	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe	PCIe

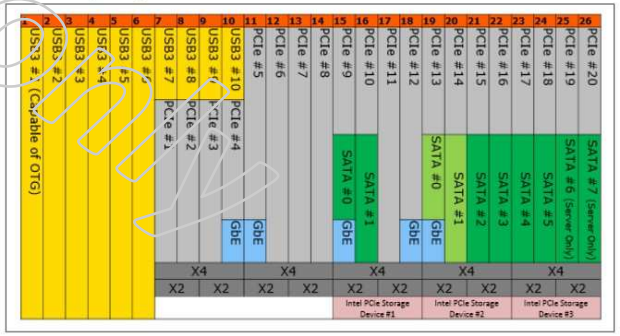
eSPI Virtual Wires (VW) (Sheet 1 of 2)

Virtual Wire	PCH Pin Direction	Reset Control	Pin Retained in PCH (For Use by Other Components)
SUS_STAT#	Output	ESPI_RESET#	No
SUS_PWRDN_ACK	Output	ESPI_RESET#	No
PLTRST#	Output	ESPI_RESET#	Yes
PME#	Input	ESPI_RESET#	No
WAKE#	Input	ESPI_RESET#	No
SMI#	Input	PLTRST#	N/A
SCI#	Input	PLTRST#	N/A
RCIN#	Input	PLTRST#	No
SLP_A#	Output	ESPI_RESET#	Yes

eSPI Virtual Wires (VW) (Sheet 2 of 2)

Virtual Wire	PCH Pin Direction	Reset Control	Pin Retained in PCH (For Use by Other Components)
SLP_S3#/SLP_S4#/ SLP_S5#/SLP_LAN#/ SLP_WLAN#	Output	DSW_PWROK	Yes

HSIO Multiplexing on PCH-H



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Issued Date	2011/08/25	Deciphered Date	2012/07/25

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Title	Notes List
Size	Document Number: LA-E992P
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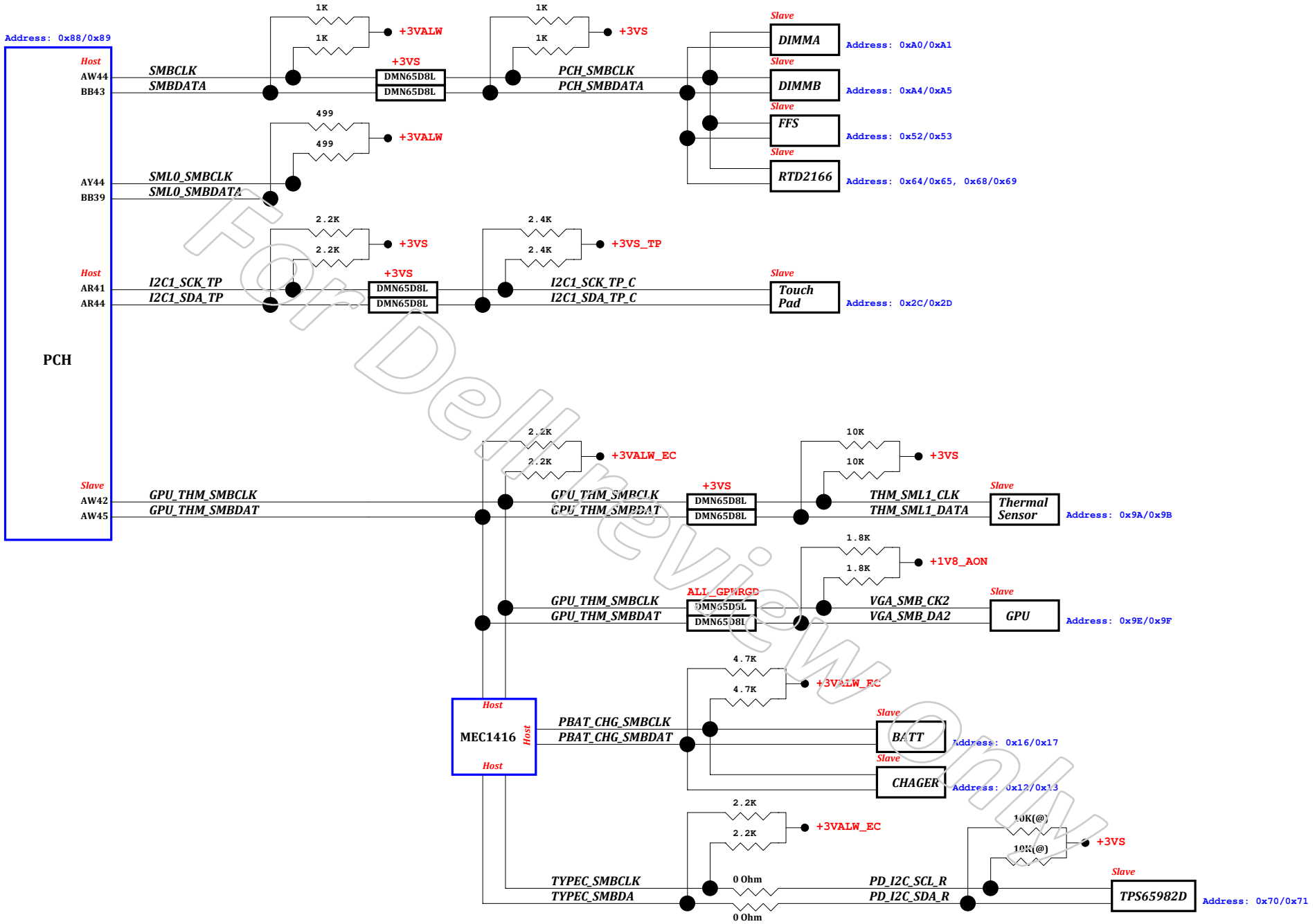

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Issued Date	2011/08/25	Deciphered Date	2012/07/15

Compal Electronics, Inc.

Title: SMBus Block Diagram

Size	Document Number	Rev
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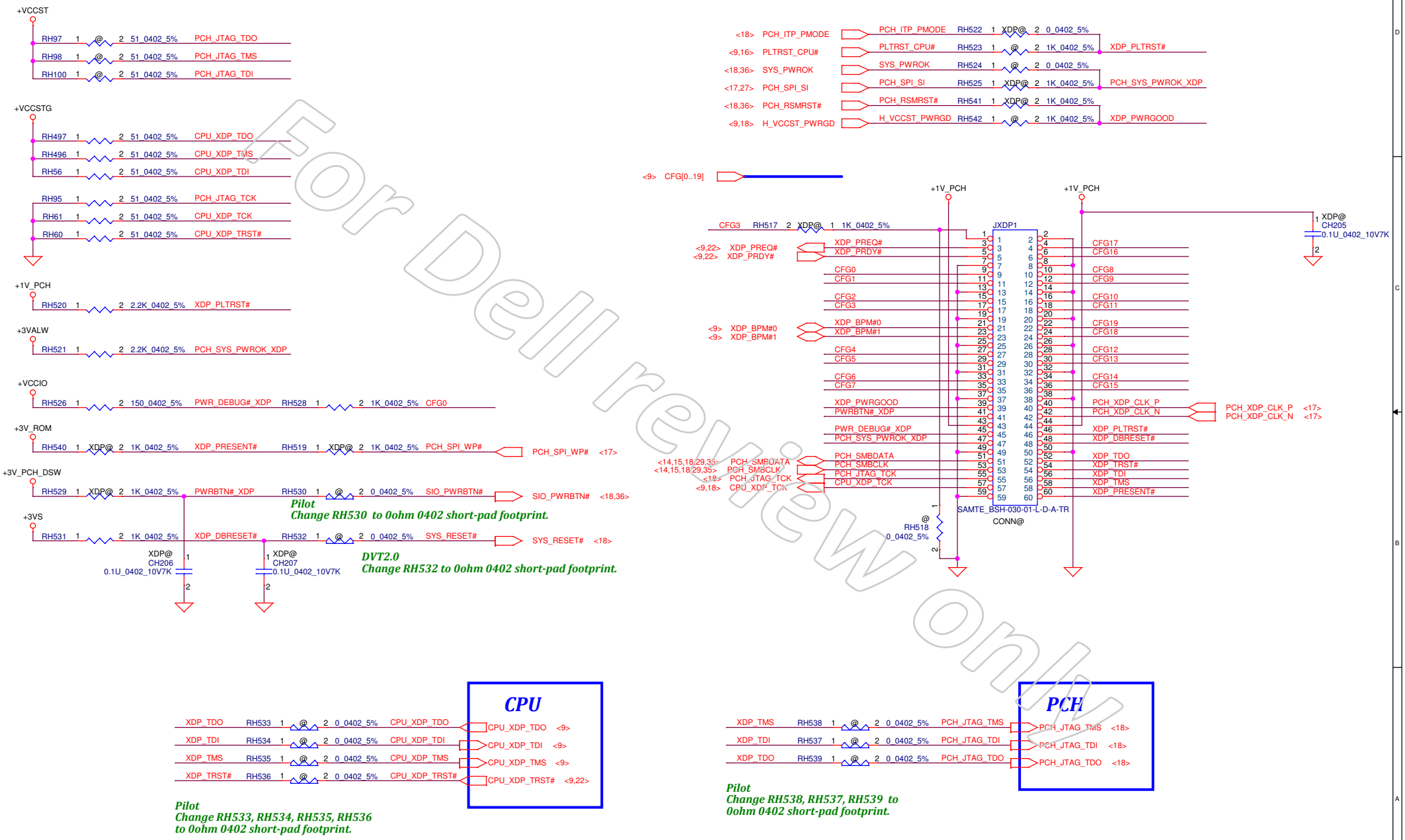

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Issued Date	2011/08/25	Deciphered Date	2012/07/25

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Title: **XDP CONN**

Size | Document Number: **LA-E992P** | Rev: 1.0(A00)

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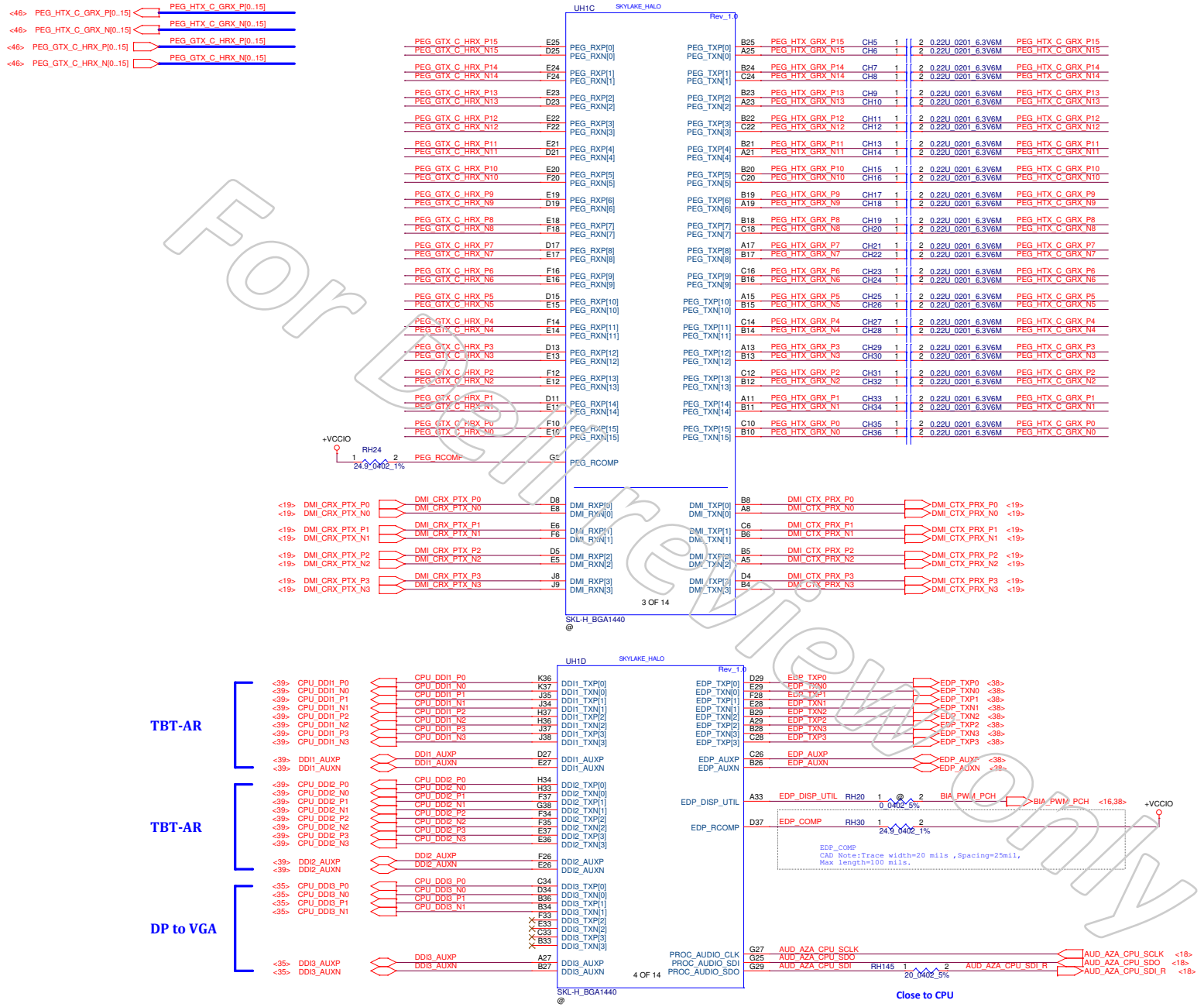

Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.			
Title	PROCESSOR(1/7) DMI,FDI,PEG		
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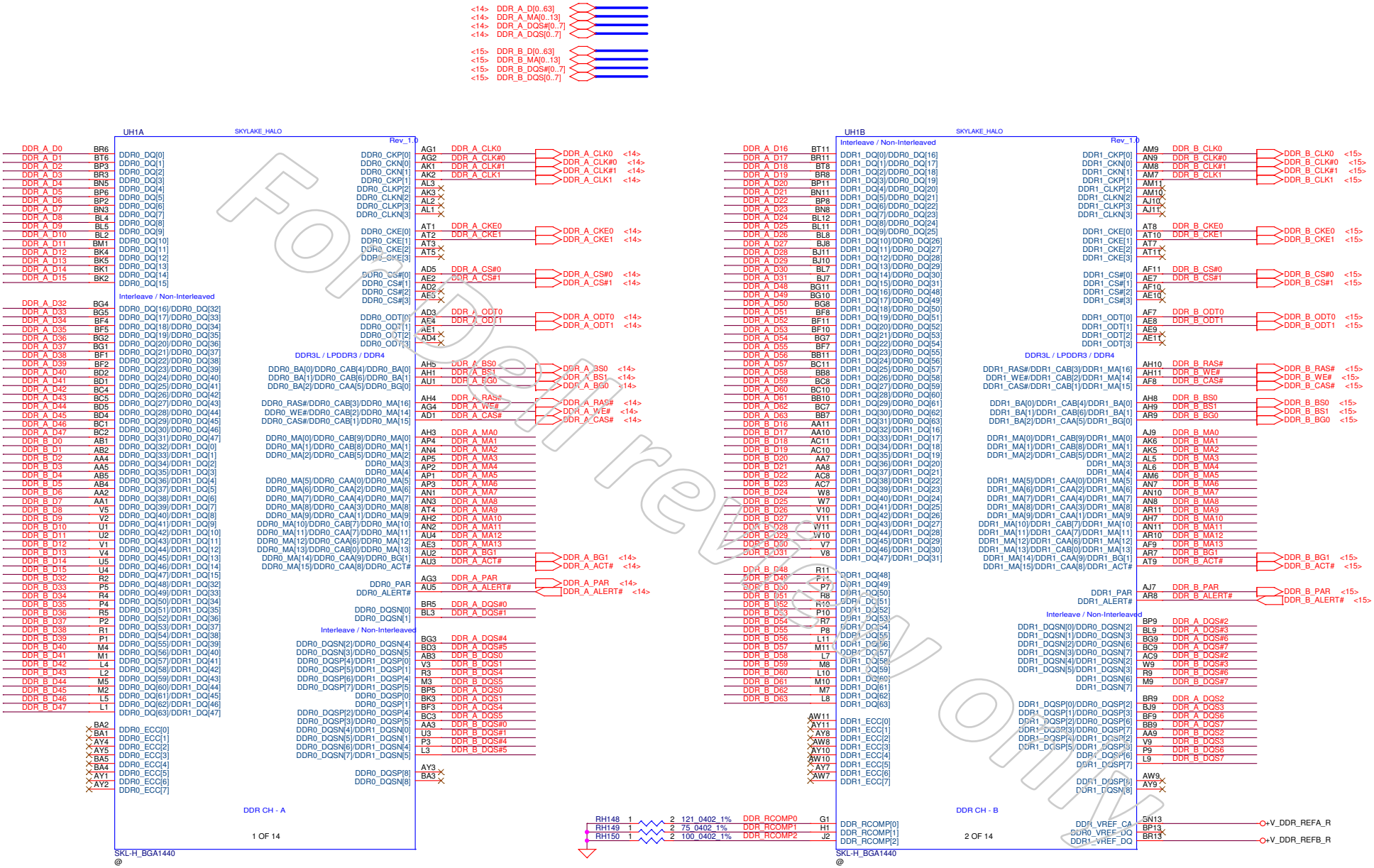
Non-Interleave



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Title	PROCESSOR(3/7) DDRIII		
Size: Custom	Document Number: LA-E992P		Rev: 1.0(A00)
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CFG Straps for Processor

Stall reset sequence after CPU PLL lock until de-asserted	
CFG0	* 1 = (Default) Normal Operation; No stall. 0 = Stall.

CFG0 RH183 1 @ 2 1K_0402_5%

PCI EXPRESS STATIC LANE REVERSAL FOR ALL PEG PORTS	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed

CFG2 RH184 1 2 1K_0402_5%

Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

CFG4 RH185 1 2 1K_0402_5%

PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

CFG5 RH186 1 @ 2 1K_0402_5%
CFG6 RH187 1 @ 2 1K_0402_5%

If change to x8, need cheange setting.

PEG DEFER TRAINING	
CFG7	* 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

CFG7 RH188 1 @ 2 1K_0402_5%

+VCCSTG
RH165 1 2 1K_0402_5% H_PROCHOT#

+VCCST
RH163 1 2 1K_0402_5% H_THERMTRIP#_R
RH156 1 @ 2 51_0402_5% XDP_PREQ#
RH164 1 2 1K_0402_5% H_VCCST_PWRGD
RH151 1 2 100_0402_5% VR_SVID_DATA
RH152 1 2 56.2_0402_1% VR_SVID_ALERT#
RH144 1 @ 2 49.9_0402_1% H_CATERR#

CFG[0..19] <6>

UH1E SKYLAKE_HALO Rev_1.0

<17> PCH_CPU_BCLK_P	PCH_CPU_BCLK_P	B31	BCLKP
<17> PCH_CPU_BCLK_N	PCH_CPU_BCLK_N	A32	BCLKN
<17> PCH_CPU_PCIBCLK_P	PCH_CPU_PCIBCLK_P	D35	PCI_BCLKP
<17> PCH_CPU_PCIBCLK_N	PCH_CPU_PCIBCLK_N	C36	PCI_BCLKN
<17> CPU_24MHZ_P	CPU_24MHZ_P	E31	CLK24P
<17> CPU_24MHZ_N	CPU_24MHZ_N	D31	CLK24N

<71> VR_SVID_ALERT#	VR_SVID_ALERT#	RH153 1 2 220_0402_5%	VR_SVID_ALERT#_R	BH31	VIDALERT#
<71> VR_SVID_CLK	VR_SVID_CLK			BH32	VIDSCK
<71> VR_SVID_DATA	VR_SVID_DATA			BH29	VIDSOUT
<36,59,60,71> H_PROCHOT#	H_PROCHOT#	RH158 1 2 499_0402_1%	H_PROCHOT#_R	BR30	PROCHOT#
	DDR_VTT_PG_CTRL			BT13	DDR_VTT_CNTL
<6,18> H_VCCST_PWRGD	H_VCCST_PWRGD	RH154 1 2 60.4_0402_1%	VCCST_PWRGD_CPU	H13	VCCST_PWRGD
<18> H_CPUPWRGD			H_CPUPWRGD	BT31	PROCPWRGD
<6,16> PLTRST_CPU#			PLTRST_CPU#	BP35	RESET#
<16> H_PM_SYNC_R			H_PM_SYNC_R	BM34	PM_SYNC
<16> H_PM_DOWN	H_PM_DOWN	RH155 1 @ 2 20_0402_5%	H_PM_DOWN_R	BP31	PM_DOWN
<16,36> PECI_EC	PECI_EC	RH190 1 @ 2 0_0402_5%	PECI_EC_R	BT34	PECI
<16> H_THERMTRIP#_R			H_THERMTRIP#_R	J31	THERMTRIP#
<16> PROC_DETECT#	PROC_DETECT#	RH89 1 @ 2 0_0402_5%		BR33	SKTOCC#
				BN1	PROC_SELECT#
	H_CATERR#			BM30	CATERR#

CFG[0]	BN25	CFG0	
CFG[1]	BN27	CFG1	
CFG[2]	BN26	CFG2	
CFG[3]	BN28	CFG3	
CFG[4]	BR20	CFG4	
CFG[5]	BM20	CFG5	
CFG[6]	BT20	CFG6	
CFG[7]	BP20	CFG7	
CFG[8]	BR23	CFG8	
CFG[9]	BR22	CFG9	
CFG[10]	BT23	CFG10	
CFG[11]	BT22	CFG11	
CFG[12]	BM19	CFG12	
CFG[13]	BR19	CFG13	
CFG[14]	BP19	CFG14	
CFG[15]	BT19	CFG15	
CFG[17]	BN23	CFG17	
CFG[16]	BP23	CFG16	
CFG[19]	BP22	CFG19	
CFG[18]	BN22	CFG18	

BPM#[0]	BR27	XDP_BPM#0
BPM#[1]	BT27	XDP_BPM#1
BPM#[2]	BM31	
BPM#[3]	BT30	

PROC_TDO	BT28	CPU_XDP_TDO	CPU_XDP_TDO <6>
PROC_TDI	BL32	CPU_XDP_TDI	CPU_XDP_TDI <6>
PROC_TMS	BP28	CPU_XDP_TMS	CPU_XDP_TMS <6>
PROC_TCK	BR28	CPU_XDP_TCK	CPU_XDP_TCK <6,18>
PROC_TRST#	BP30	CPU_XDP_TRST#	CPU_XDP_TRST# <6,22>
PROC_PREQ#	BL30	XDP_PREQ#	XDP_PREQ# <6,22>
PROC_PRDY#	BP27	XDP_PRDY#	XDP_PRDY# <6,22>

CFG_RCOMP BT25 CFG_RCOMP
RH59 49.9_0402_1%

5 OF 14
SKL-H_BGA1440
@

DVT2.0
Change RH190 to 0ohm 0402 short-pad footprint.

+1.2V_DDR
CH197 0.1U_0402_10V7K
+3VS
RH93 220K_0402_5%
UC1 74AUP1G07SE-7_SOT353
VCC NC A GND
DDR_VTT_PG_CTRL
<62> SM_PG_CTRL
SM_PG_CTRL
SA00007VE00

Reserve for ESD

H_VCCST_PWRGD CH210 1 2 @ESD@ 100P_0402_50V8J
H_PROCHOT#_R CH211 1 2 100P_0402_50V8J

UH1K SKYLAKE_HALO Rev_1.0

D1	RSVD_TP	BM33	RSVD_TP
E1	RSVD_TP	BL33	RSVD_TP
E3	RSVD_TP	BJ14	RSVD_TP
E2	RSVD_TP	BJ13	RSVD_TP
BR1	RSVD_TP	BK28	RSVD
BT2	RSVD_TP	BJ28	RSVD
BN35	RSVD	BJ18	VSS
J24	RSVD	BJ16	RSVD_TP
H24	RSVD	BK16	RSVD_TP
BN33	RSVD	BK24	RSVD_TP
BL34	RSVD	BJ24	RSVD_TP
N29	RSVD	BK21	RSVD
R14	RSVD	BJ21	RSVD
AE29	RSVD	BT17	RSVD
AA14	RSVD	BR17	RSVD
A36	RSVD	BK18	VSS
A37	RSVD	BJ34	RSVD_TP
		BJ33	RSVD_TP
F30	RSVD	G13	RSVD
E30	RSVD	AJ8	RSVD
B30	RSVD	BL31	RSVD
C30	RSVD	B2	NCTF
G3	RSVD	B38	NCTF
J3	RSVD	BP1	NCTF
BR35	RSVD	BR2	NCTF
BR31	RSVD	C1	NCTF
BH30	RSVD	C38	NCTF

PROC_TRIGIN	PCH_TRIGGER	RH167 1 2 30_0402_5%	PCH_TRIGGER_R
PROC_TRIGOUT	CPU_TRIGGER	RH192 1 2 30_0402_5%	CPU_TRIGGER_R

<22> PCH_TRIGGER
<22> CPU_TRIGGER

11 OF 14
SKL-H_BGA1440
@

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Issued Date	2011/08/25	Deciphered Date	2012/07/25

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Title: PROCESSOR(4/7) RSVD,CFG

Size: Custom	Document Number: LA-E992P	Rev: 1.0(A00)
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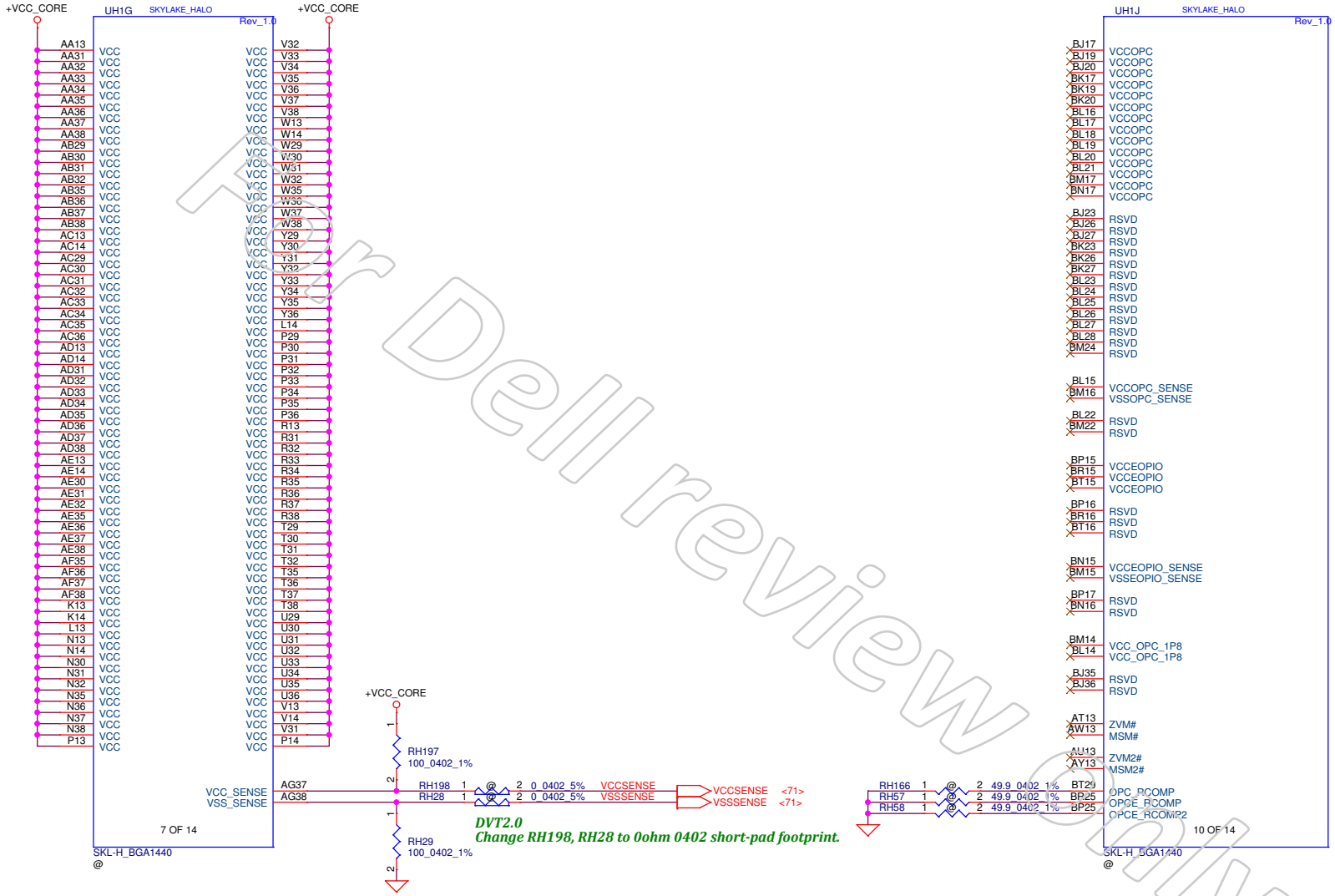

Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Title: **PROCESSOR(5/7) PWR,BYPASS**

Size	Document Number	Rev
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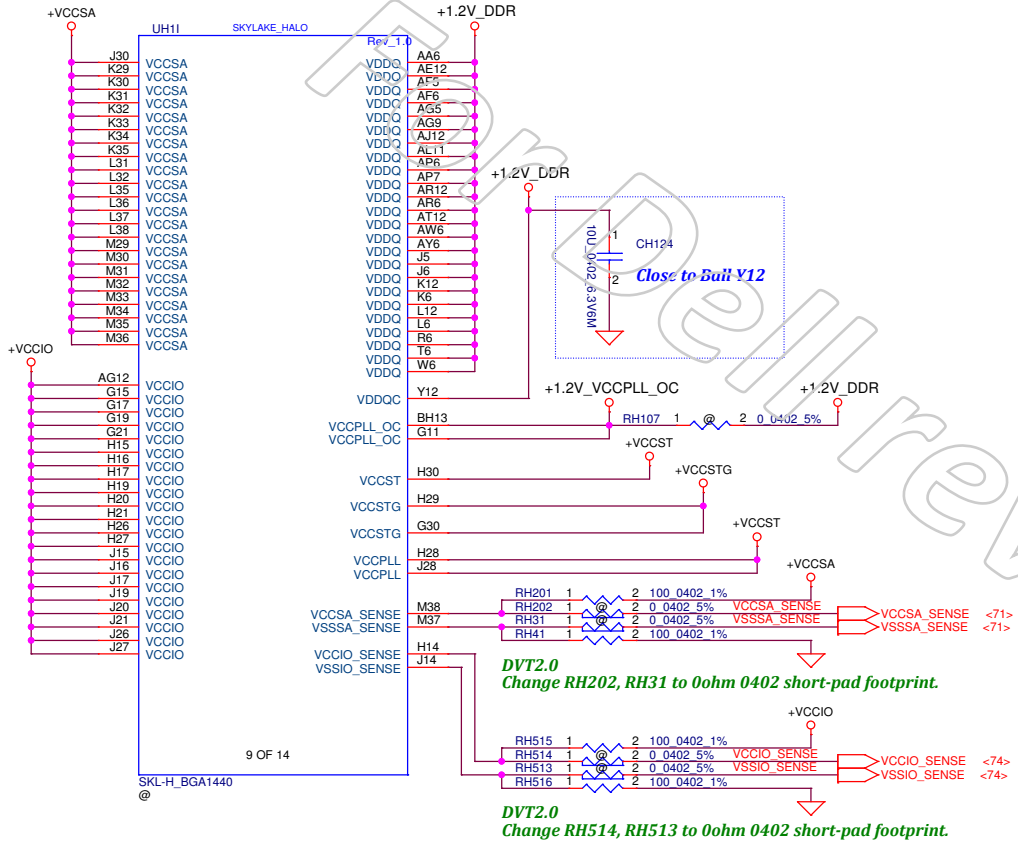

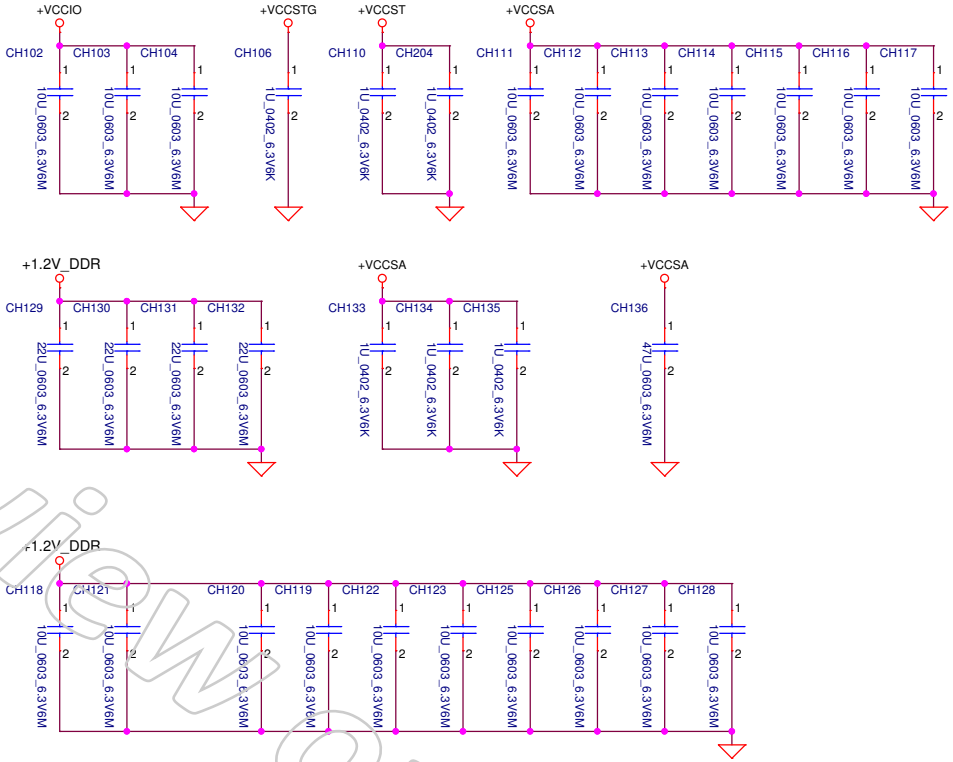

Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

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Title: PROCESSOR(6/7) PWR

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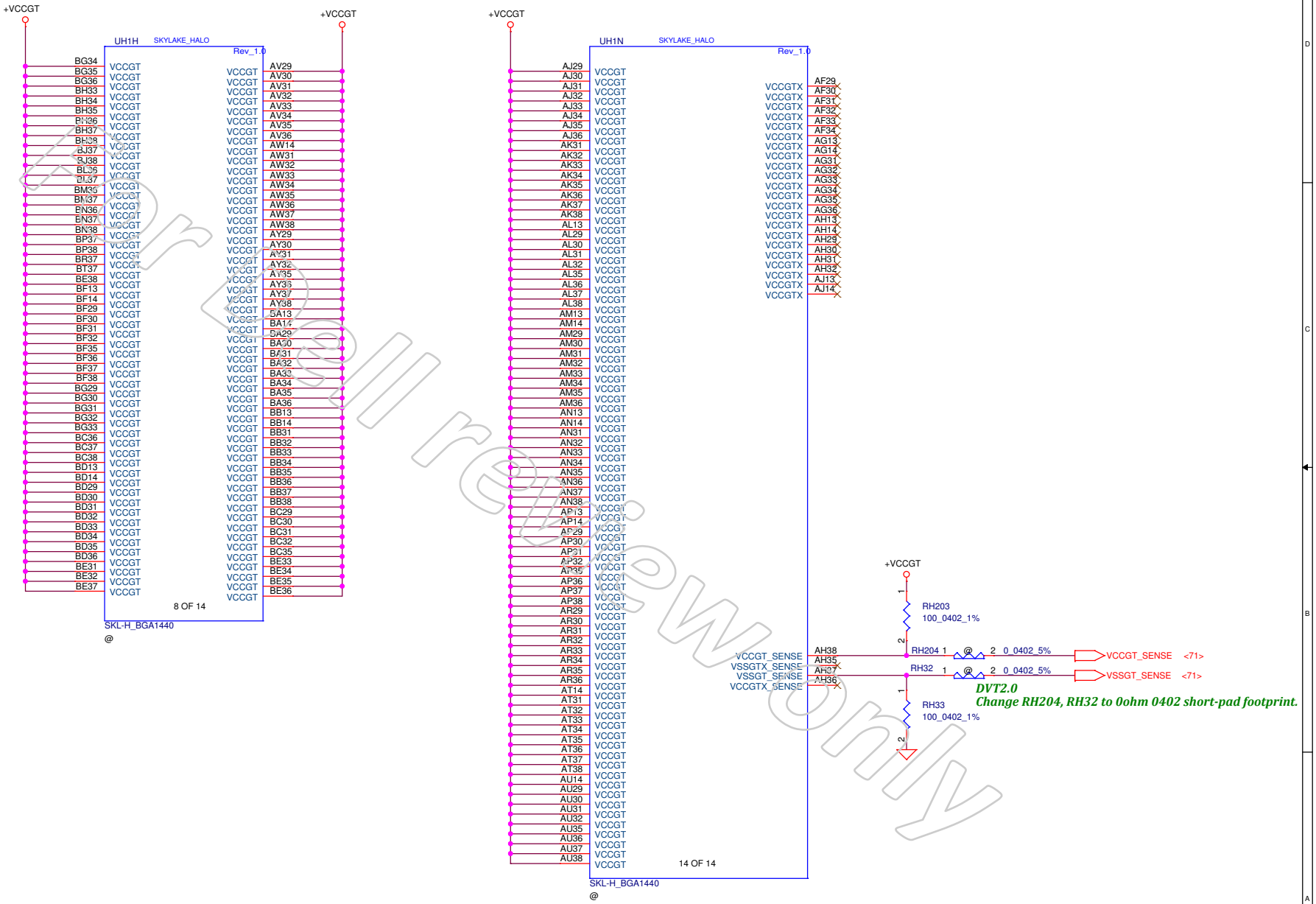

Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Title: **PROCESSOR(2/7) PM,XDP,CLK**

Size	Document Number	Rev
Custom	LA-E992P	1.0(A00)

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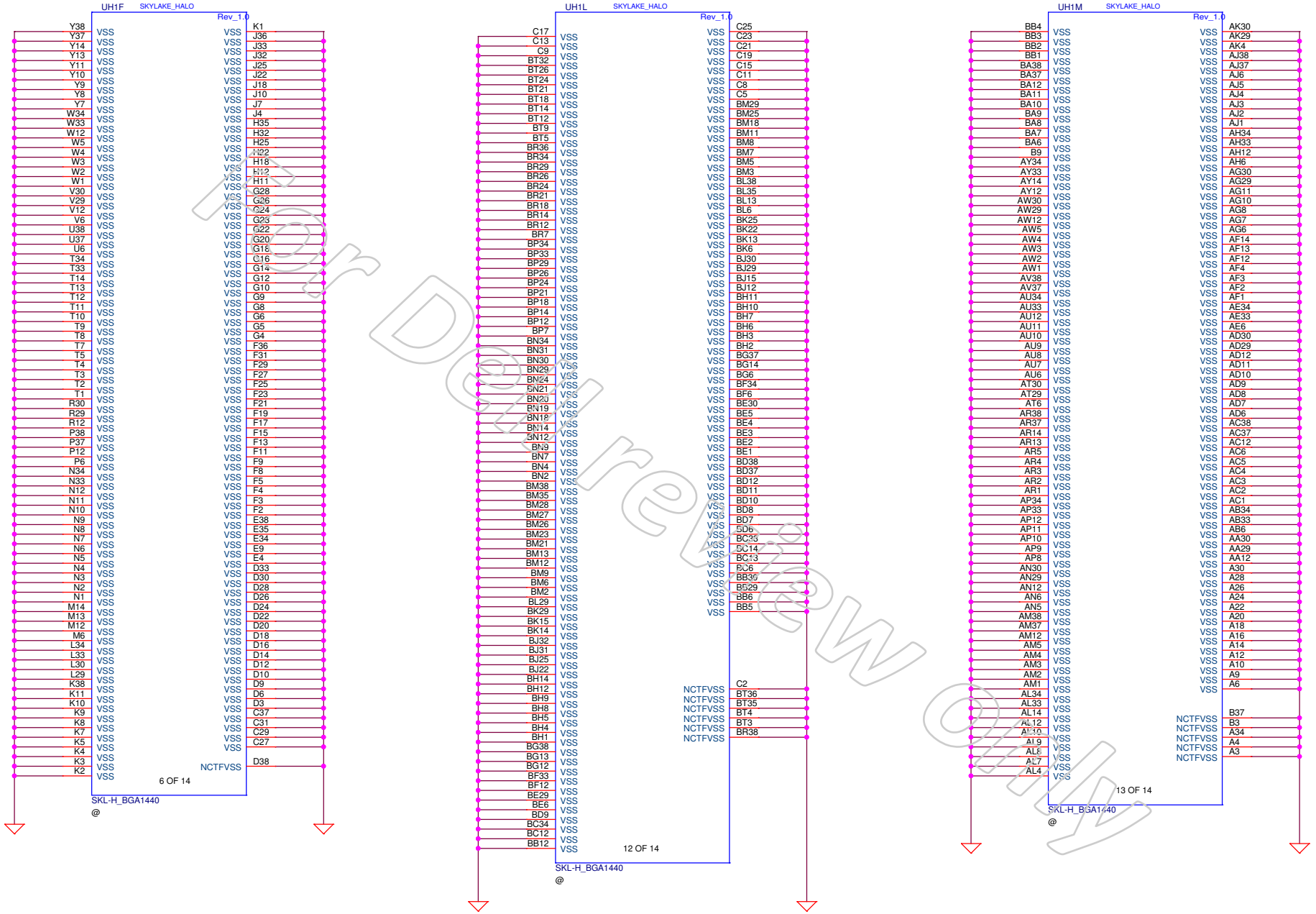

Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Title: **PROCESSOR(7/7) VSS**

Size: Custom | Document Number: **LA-E992P** | Rev: 1.0(A00)

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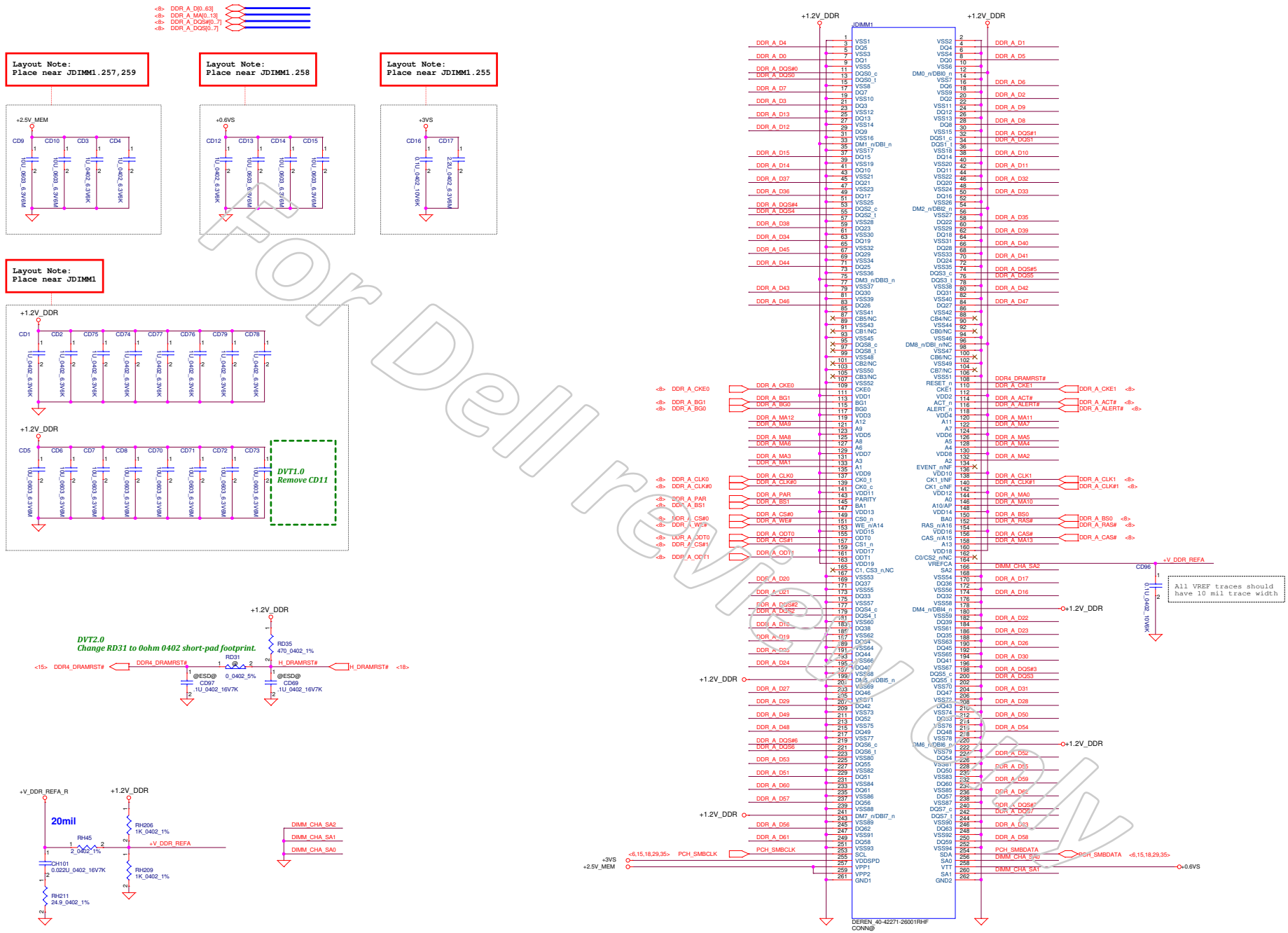

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/08/25	Deciphered Date 2012/07/25	Title: DDRIII DIMMA
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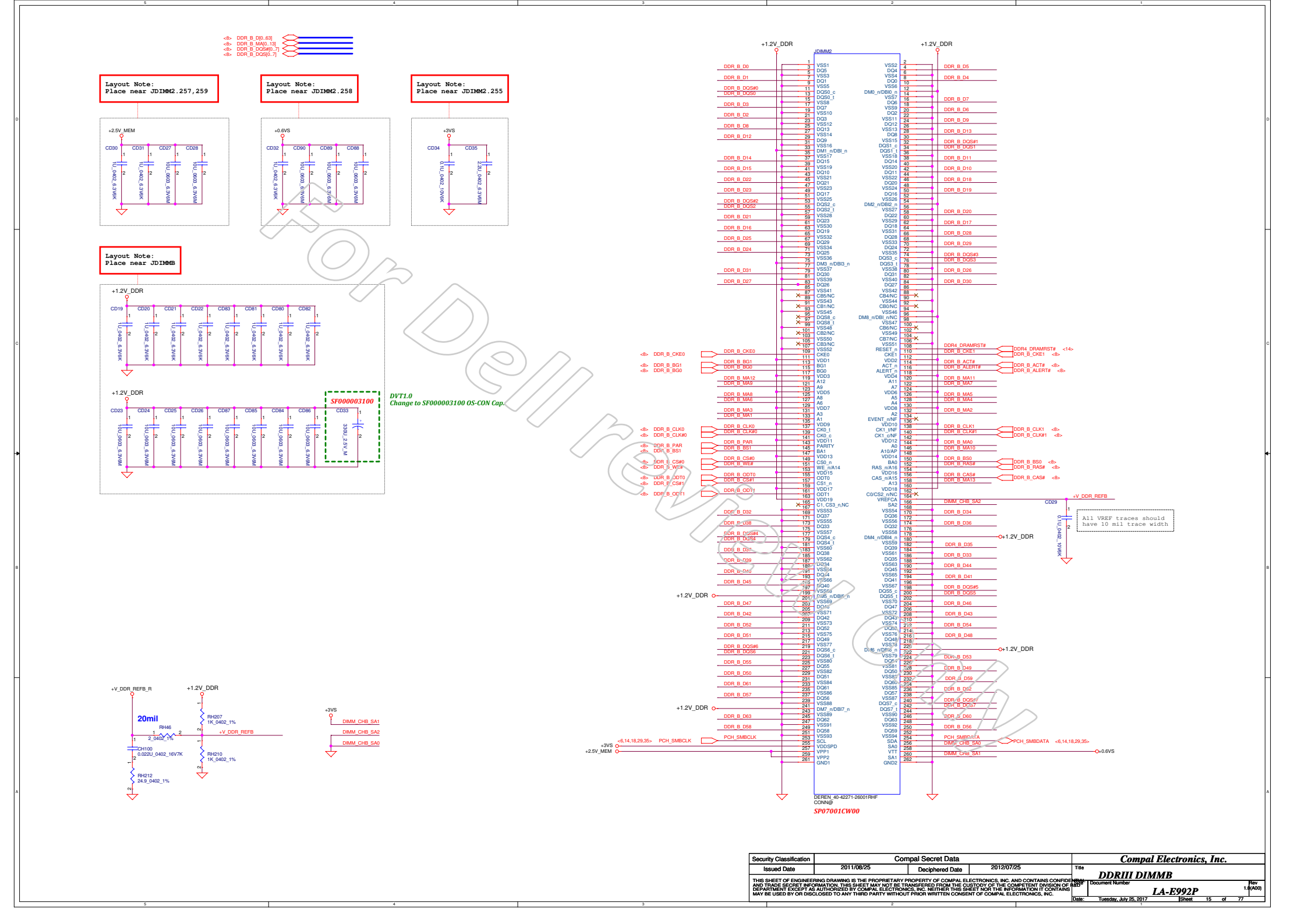

Security Classification	Compal Secret Data		Compal Electronics, Inc.
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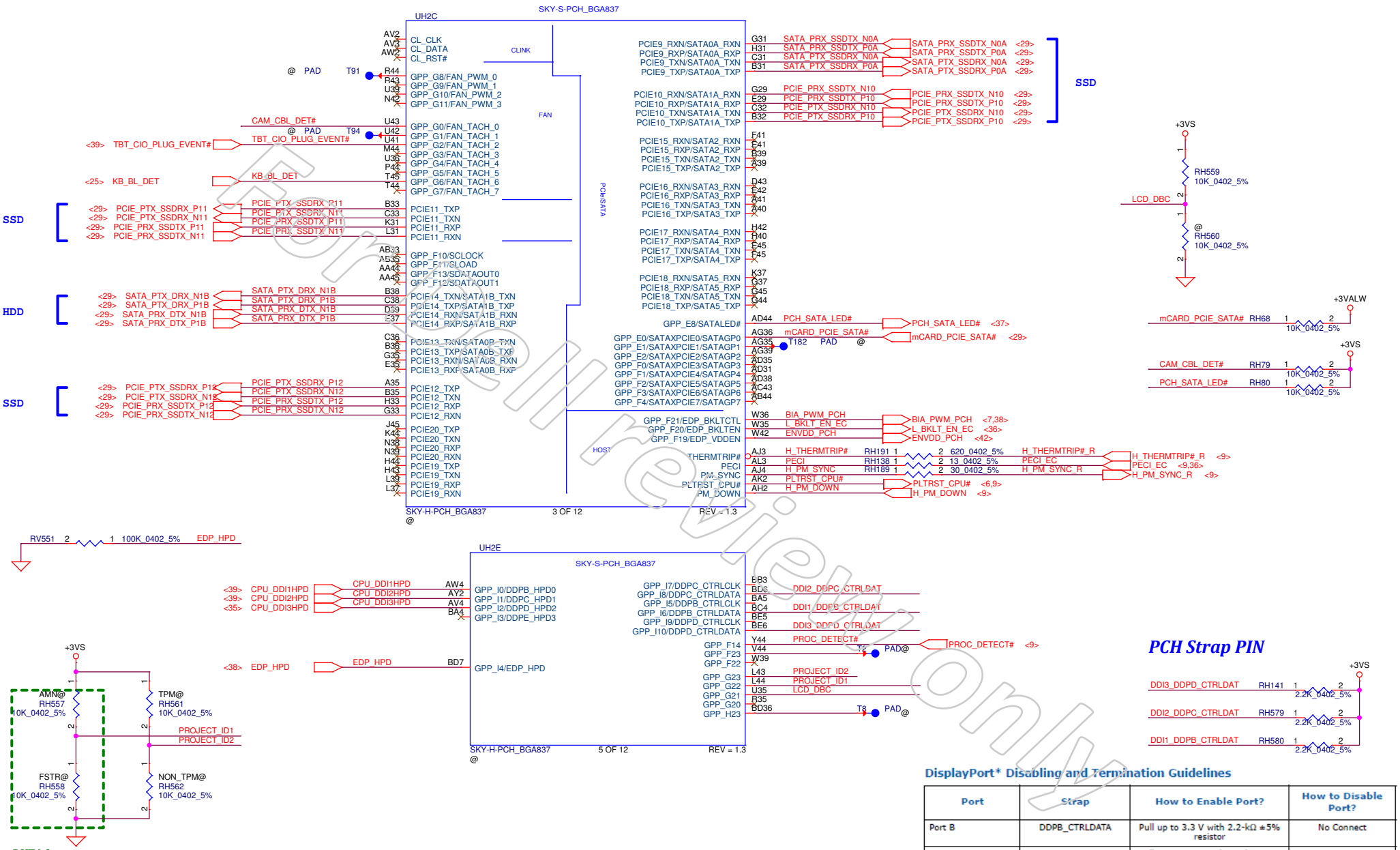
Document Number	LA-E992P	Rev 1.0(A00)	
Date: Tuesday, July 25, 2017	Sheet 15 of 77		



DVT1.0
Change RH557 BS to AMN@.
Change RH558 BS to FSTR@

PROJECT ID	PROJECT ID1 (GPP_G22)
Firestar	0
Armani	1

TPM ID	PROJECT ID2 (GPP_G23)
SW TPM	0
HW TPM	1

DisplayPort* Disabling and Termination Guidelines

Port	Strap	How to Enable Port?	How to Disable Port?
Port B	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port C	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port D	DDPD_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect

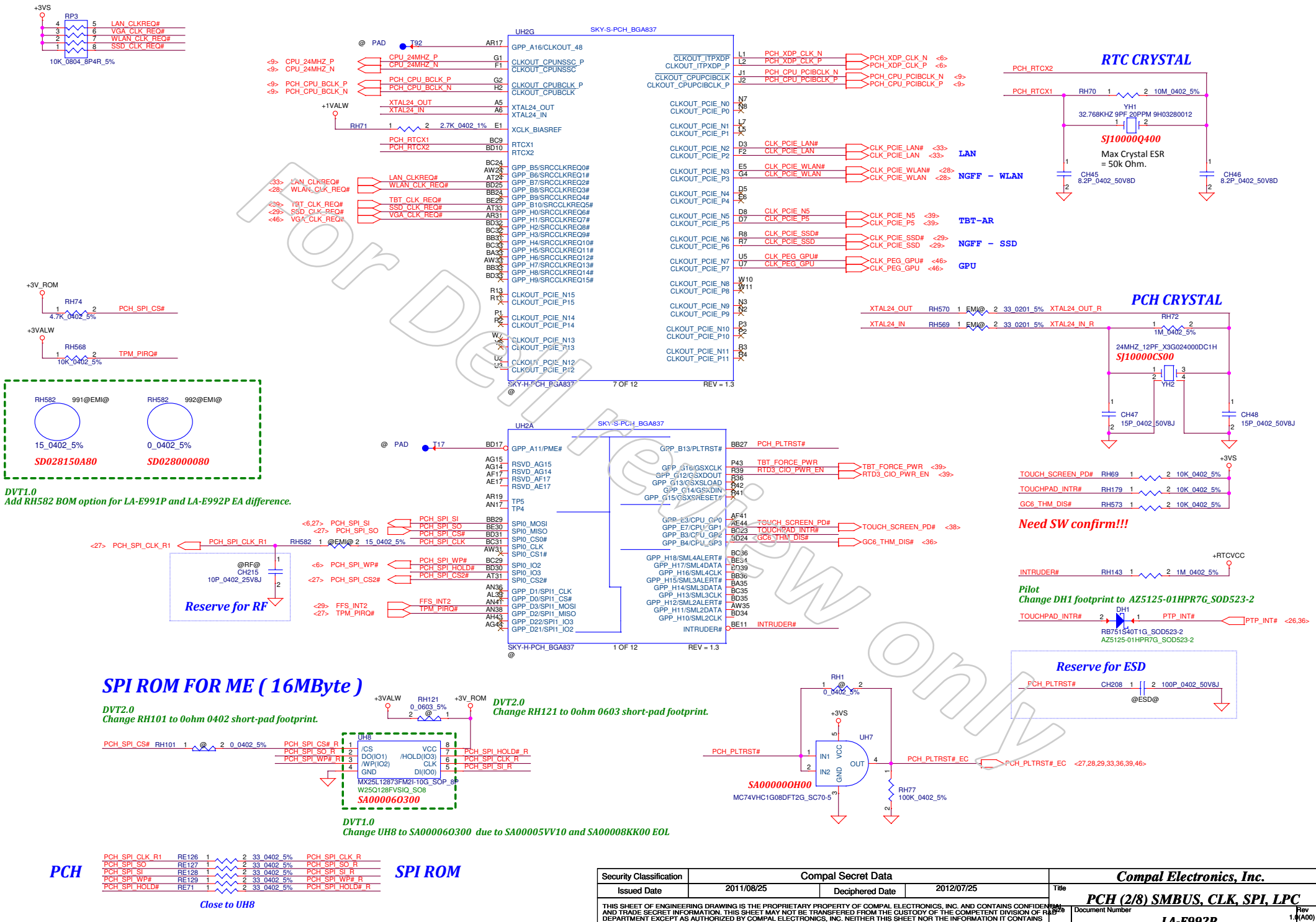
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: PCH (1/8) SATA,HDA

Size | Document Number: LA-E992P | Rev: 1.0(A00)

Date: Tuesday, July 25, 2017 | Sheet 16 of 77



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

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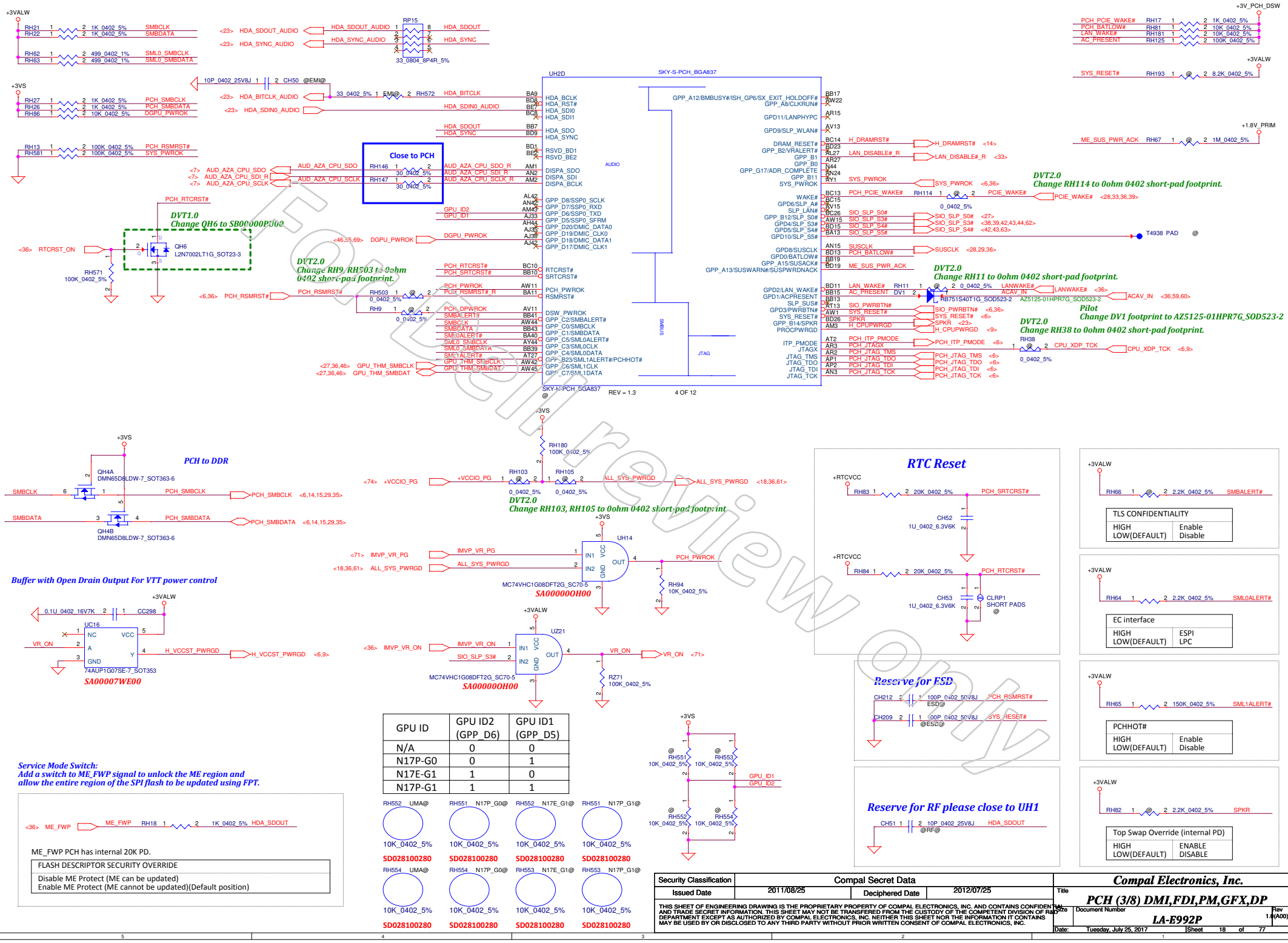
Compal Electronics, Inc.

Title: PCH (2/8) SMBUS, CLK, SPI, LPC

Size: | Document Number: LA-E992P | Rev: 1.0(A00)

Date: Tuesday, July 25, 2017 | Sheet 17 of 77



GPU ID	GPU ID2 (GPP_D6)	GPU ID1 (GPP_D5)
N/A	0	0
N17P-G0	0	1
N17E-G1	1	0
N17P-G1	1	1

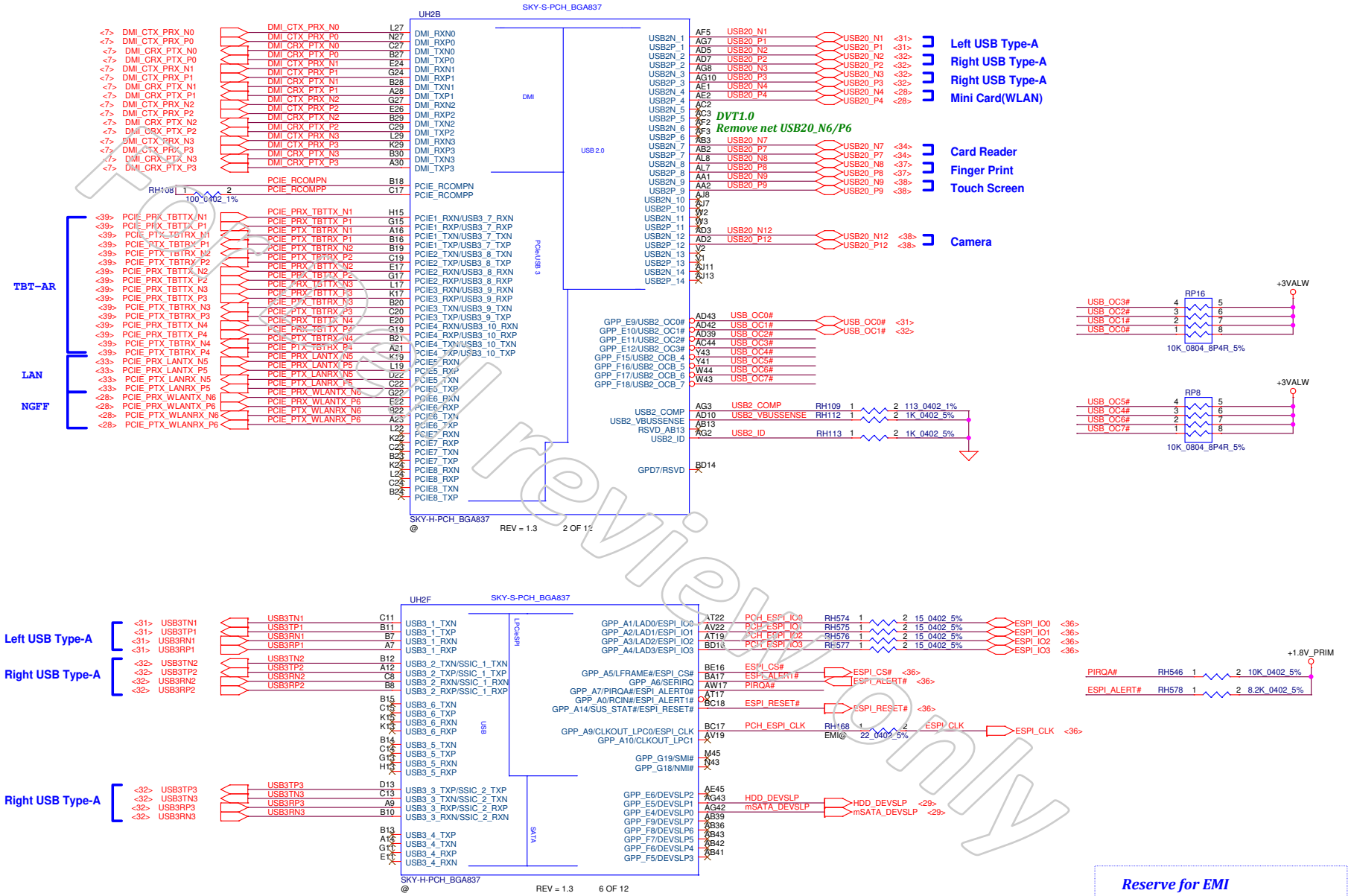
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

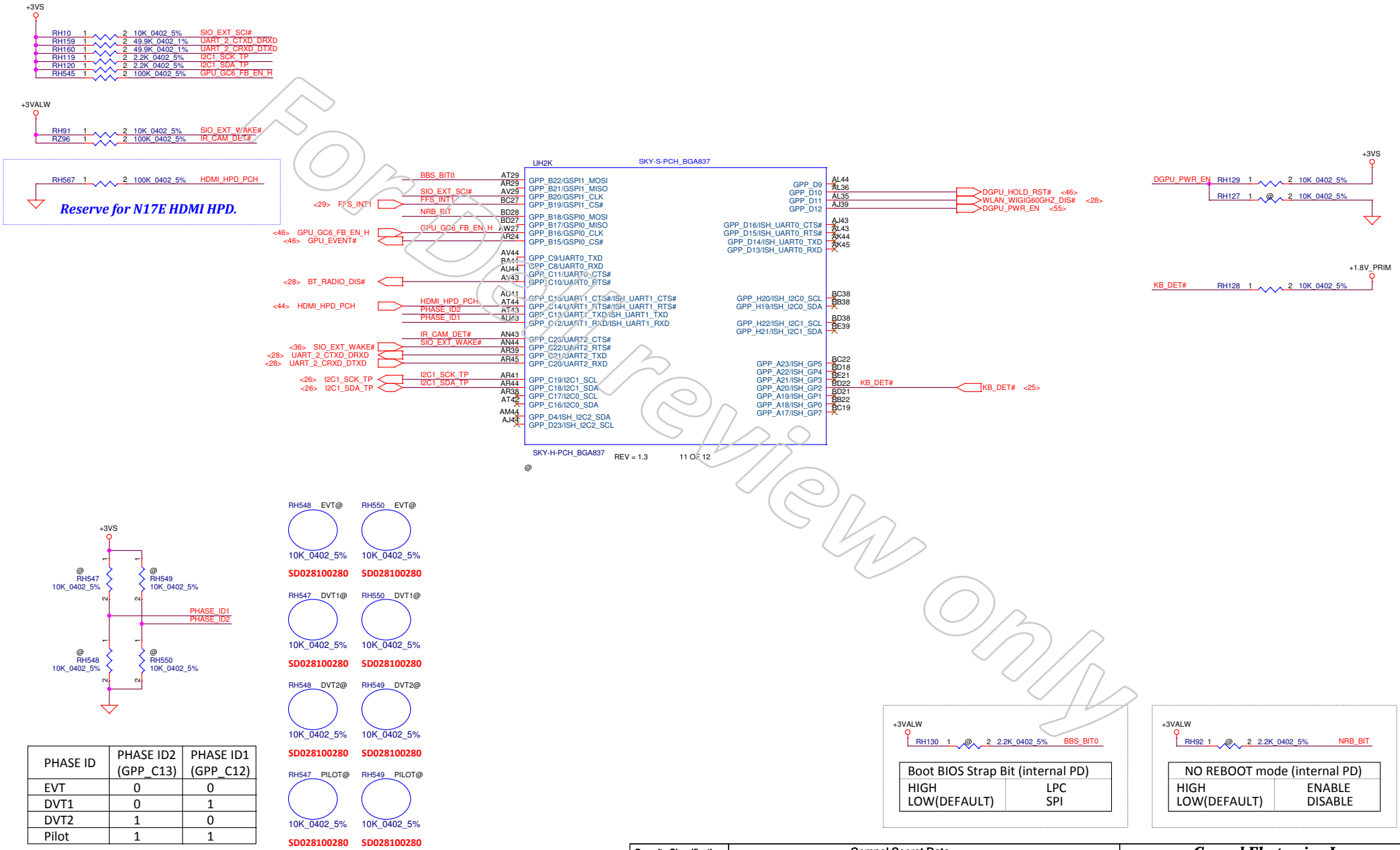
Title: PCH (3/8) DMI,FDI,PM,GFX,DP

Size: | Document Number: LA-E992P | Rev: 1.0(A00)

Date: Tuesday, July 25, 2017 | Sheet 18 of 77



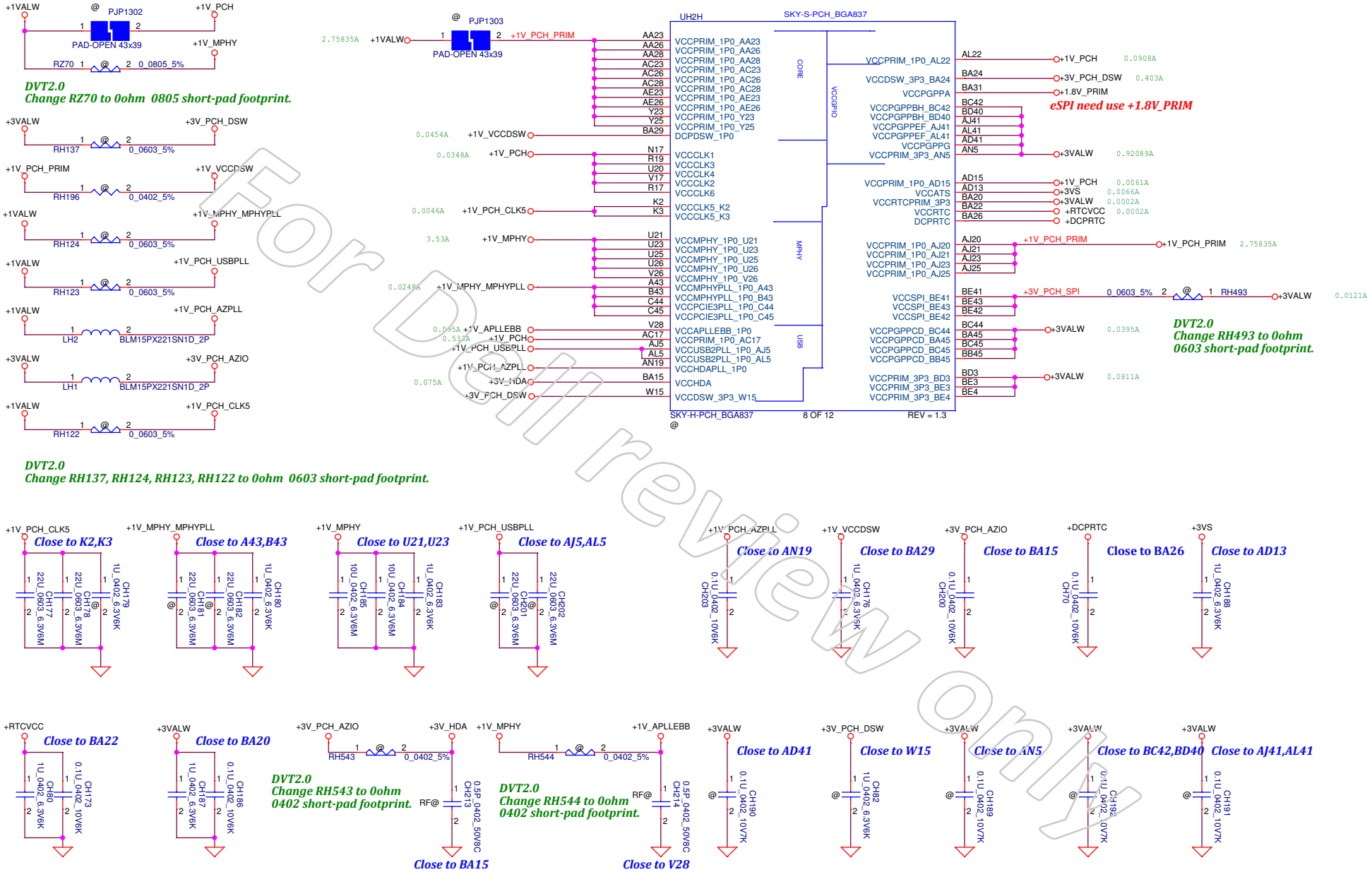
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/08/25	Deciphered Date 2012/07/25	Title: PCH (4/8) PCI, USB
			Size: B — Document Number: LA-E992P — Rev: 1.0(A00)
			Date: Tuesday, July 25, 2017 — Sheet 19 of 77



PHASE ID	PHASE ID2 (GPP_C13)	PHASE ID1 (GPP_C12)
EVT	0	0
DVT1	0	1
DVT2	1	0
Pilot	1	1

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/08/25	Deciphered Date 2012/07/25	Title: PCH (5/8) GPIO, CPU, MISC

Size	Document Number		Rev
B	LA-E992P		1.0(A00)
Date: Tuesday, July 25, 2017	Sheet 20 of 77		



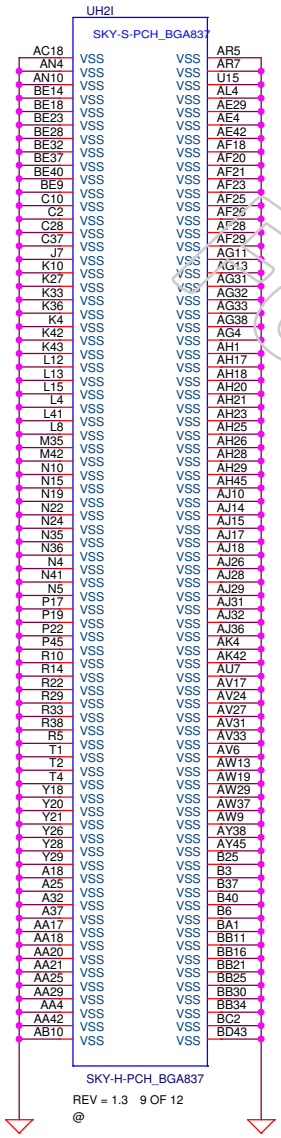
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

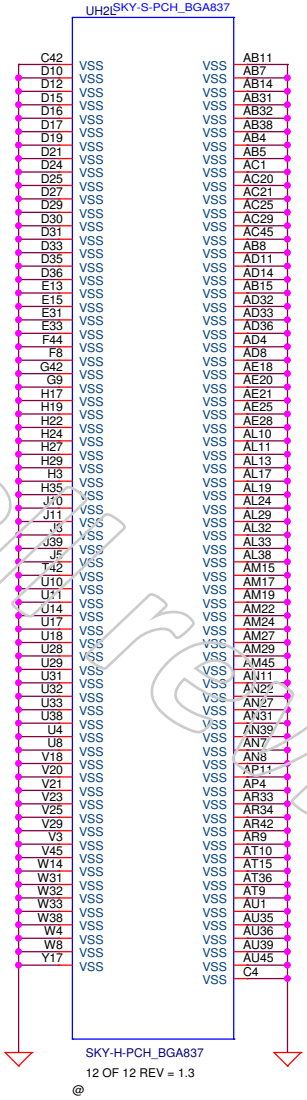
Compal Electronics, Inc.

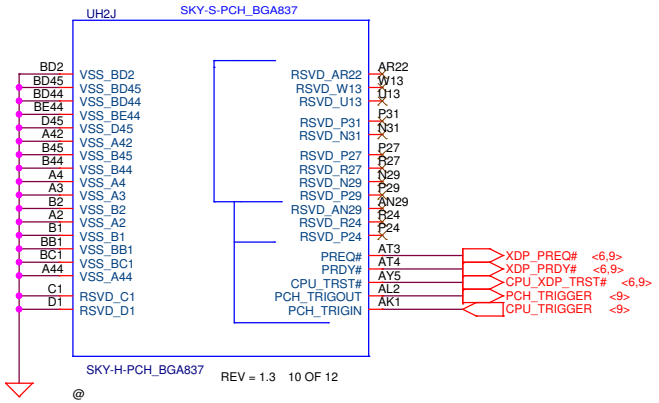
Title: **PCH (6/8) PWR**

Size | Document Number: **LA-E992P** | Rev: 1.0(A00)

Date: Tuesday, July 25, 2017 | Sheet 21 of 77







Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: **PCH (8/8) VSS**

Size | Document Number: **LA-E992P** | Rev: 1.0(A00)

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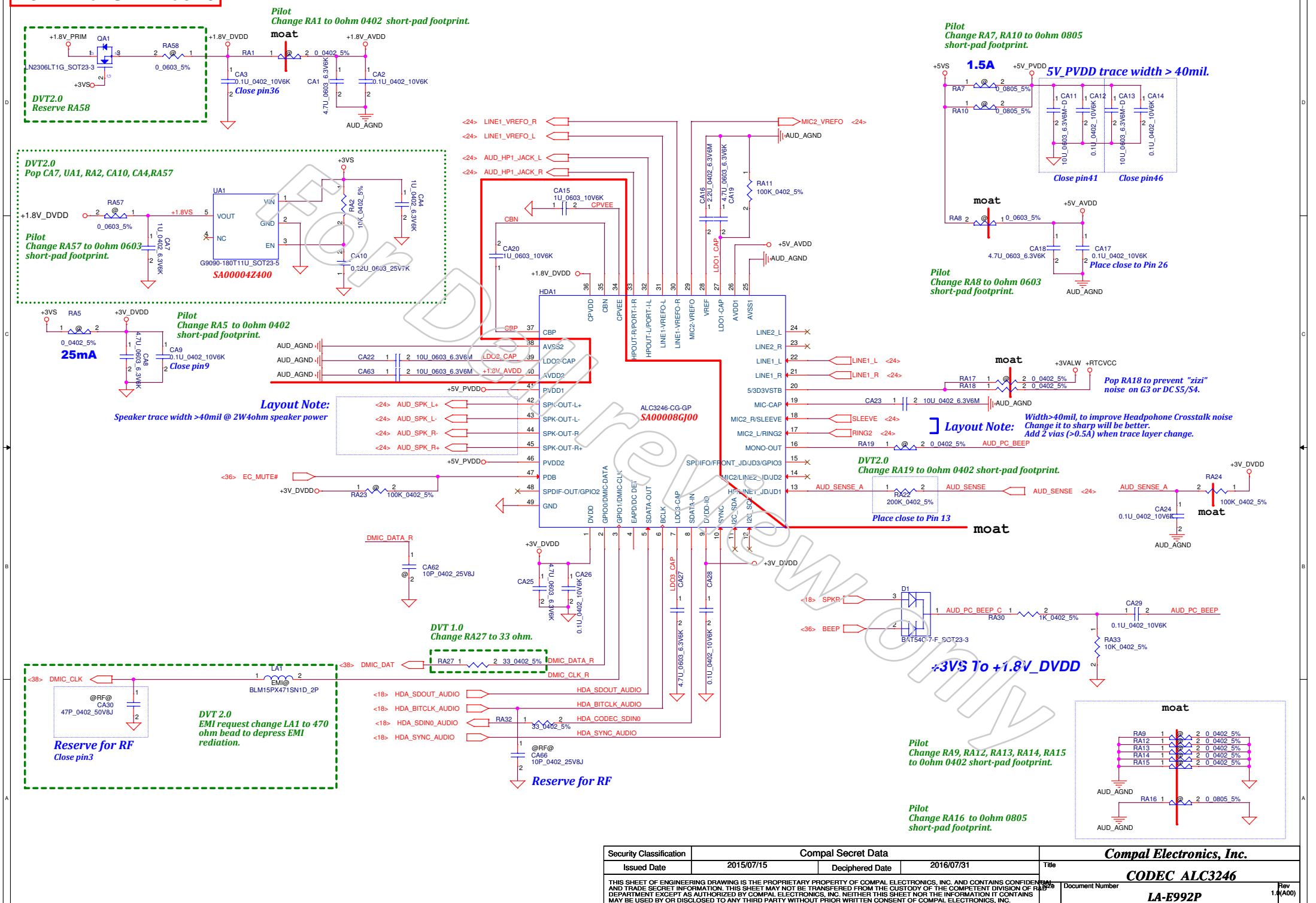
Main Func = Audio



Security Classification	Compal Secret Data		
Issued Date	2015/07/15	Deciphered Date	2016/07/31

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Compal Electronics, Inc.

Title: **CODEC ALC3246**

Size: | Document Number: **LA-E992P** | Rev: 1.0(A00)

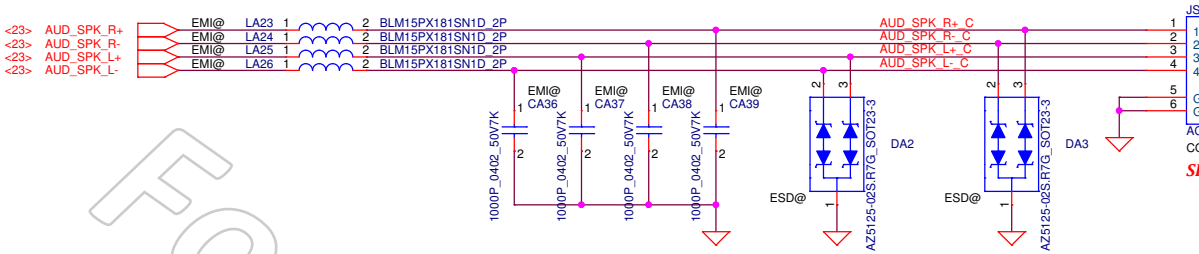
Date: Tuesday, July 25, 2017 | Sheet 23 of 77

Main Func = Audio

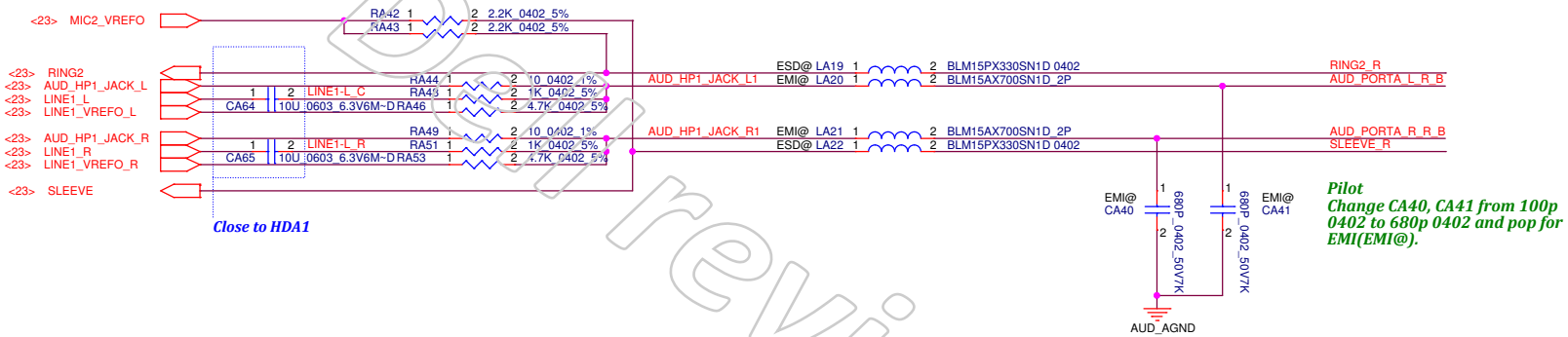
Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power

Need to check Speaker pin define

Speaker

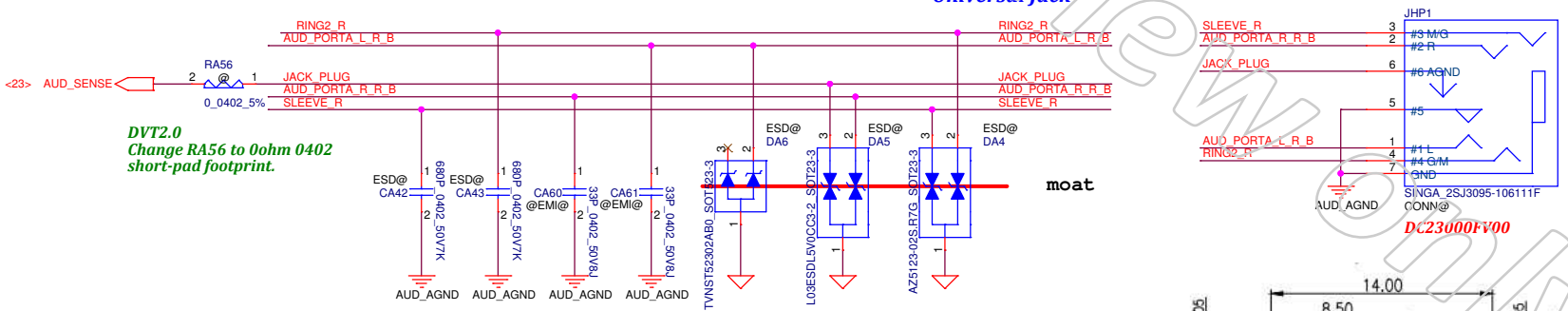


CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L-



Pilot
Change CA40, CA41 from 100p 0402 to 680p 0402 and pop for EMI(EMI@).

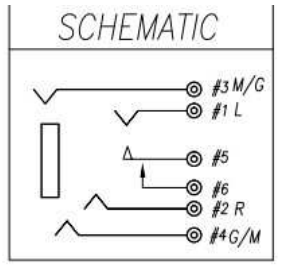
Universal Jack

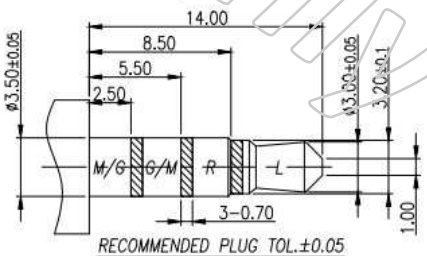


DVT2.0
Change RA56 to 0ohm 0402 short-pad footprint.

DC23000FV00

SINGA_2SJ3095-106111F





Pilot
Change connect CA42.2, CA43.2, CA60.2, CA61.2 from GND to AGND.
Change CA60, CA61 BS from EMI@ to @EMI@ reserve for EMI.

10 mils 10 mils

Security Classification	Compal Secret Data		
Issued Date	2015/07/15	Deciphered Date	2016/07/31

Compal Electronics, Inc.

Title: **SPKR/JACK**

Size | Document Number: **LA-E992P** | Rev: 1.0(A00)

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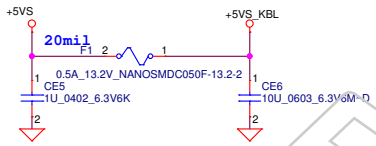
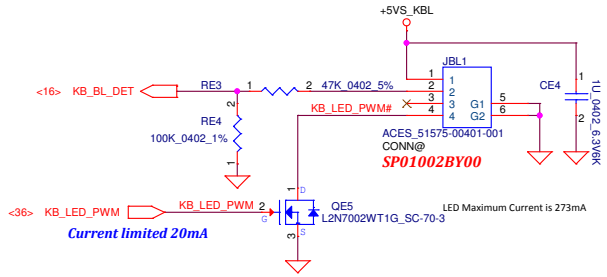
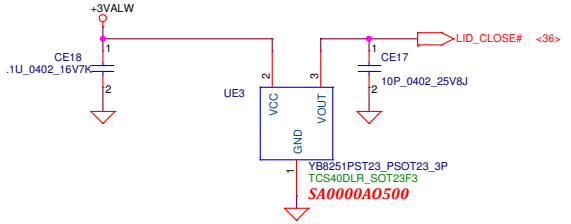
Fuse for Backlight



Connector for Keyboard Backlight

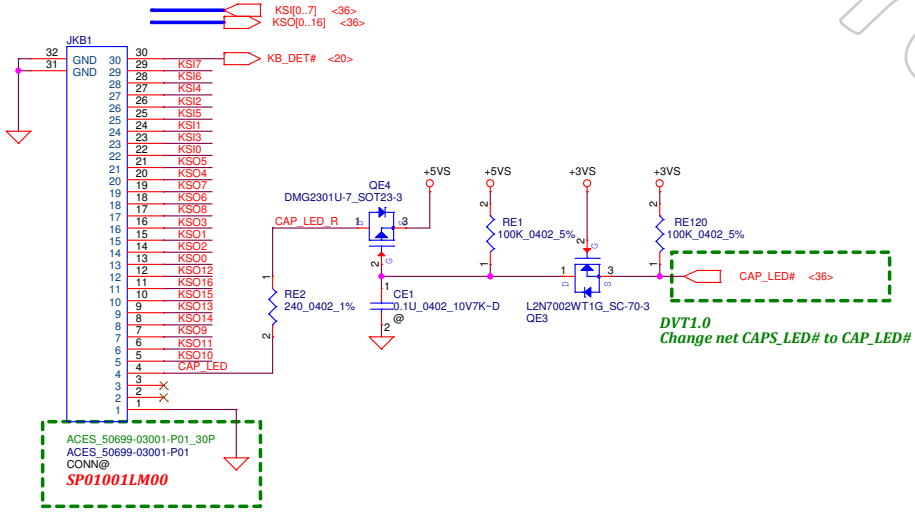


Lid Switch



Pilot
Change UE3 from SA00009CB00 TCS40DLR to SA0000AO500 YB8251PST23

Connector for Keyboard



DVT1.0
Change net CAPS_LED# to CAP_LED#

DVT1.0
Change to symbol ACES_50699-03001-P01

Connector for Touch Finger Print module. (Cancel)

DVT1.0
Remove Finger print connector and component.

Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

Compal Electronics, Inc.			
Title: KB/Lid/Finger Print			
Size	Document Number: LA-E992P		Rev: 1.0(A00)
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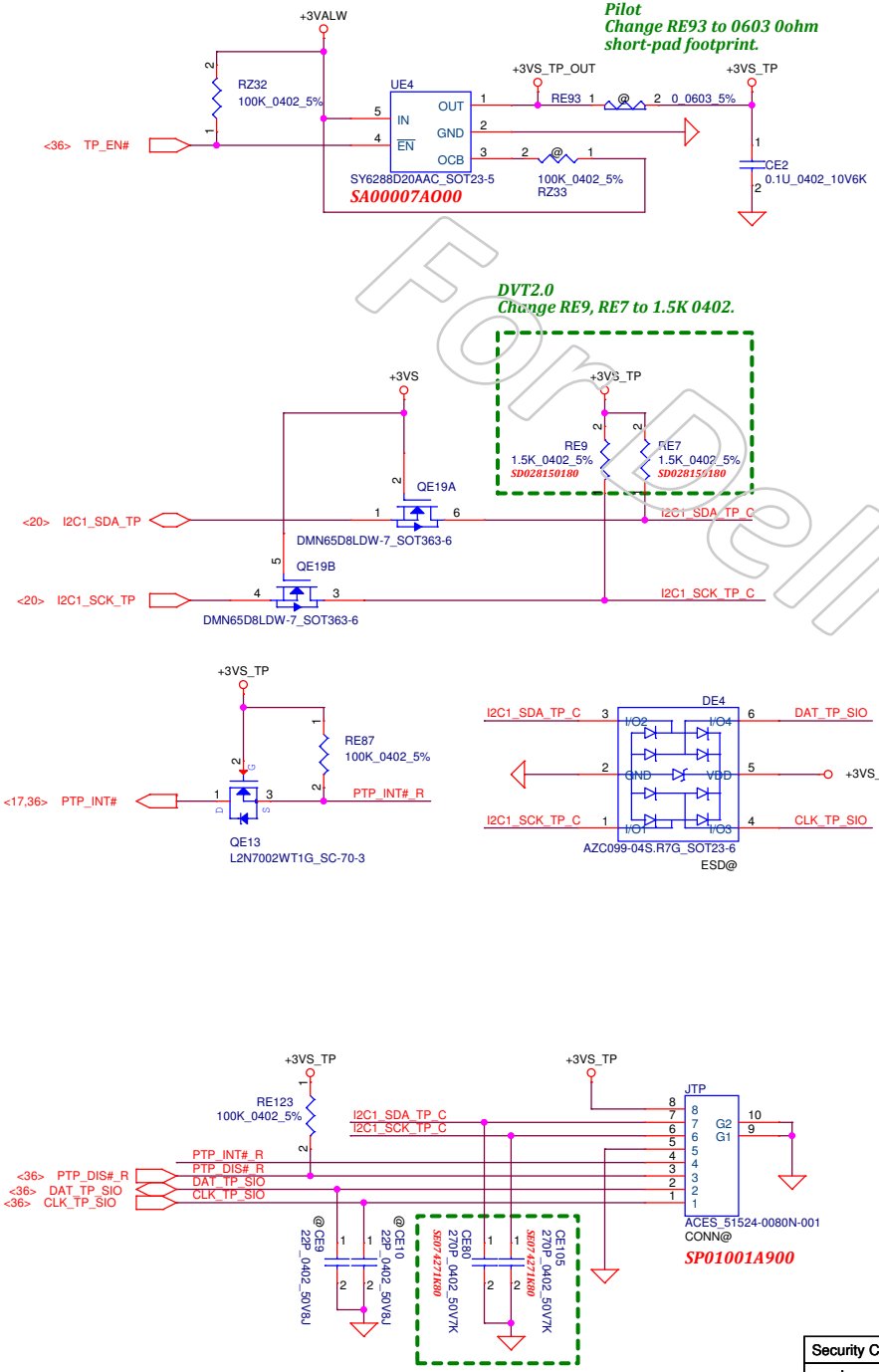
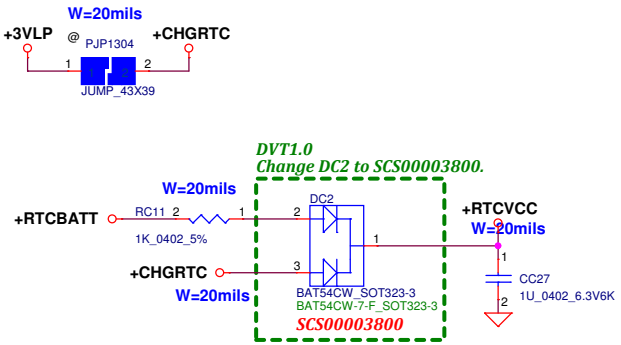
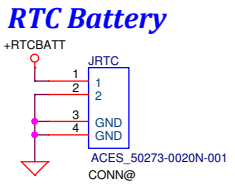
Touch pad



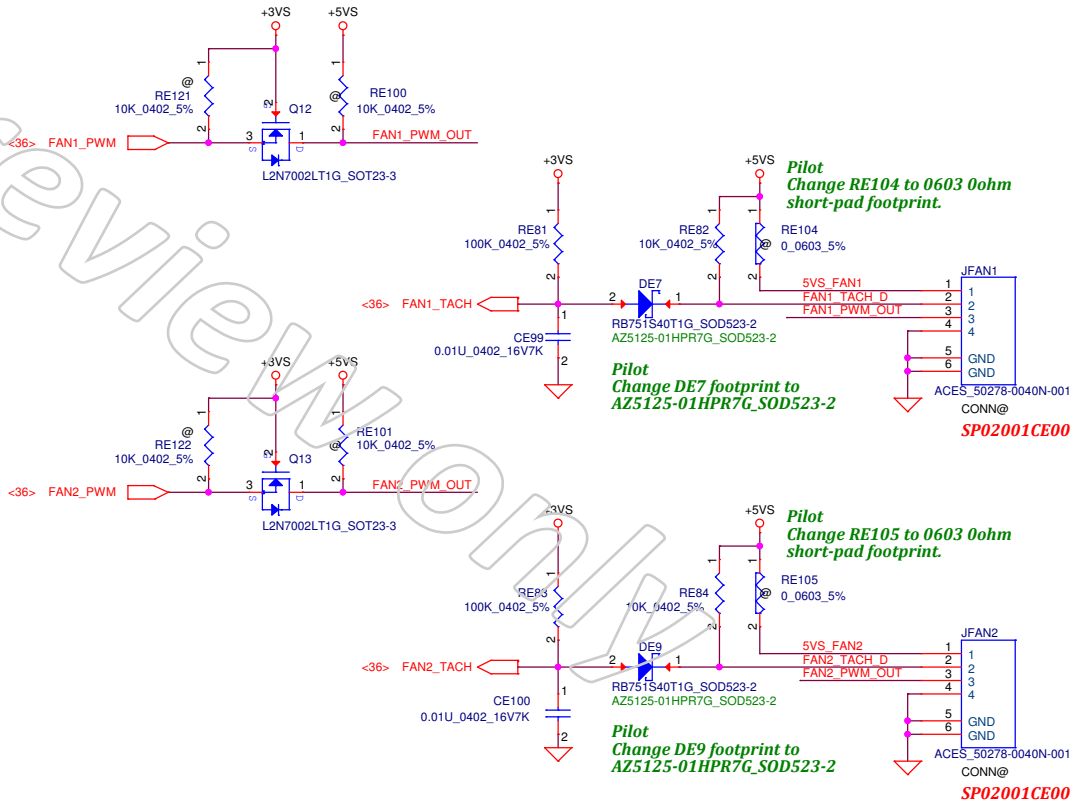
RTC Battery non- Charge Function



RTC Battery



PWM FAN



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: **FAN/TP/KB/PWR SW**

Size: Custom | Document Number: **LA-E992P** | Rev: 1.0(A00)

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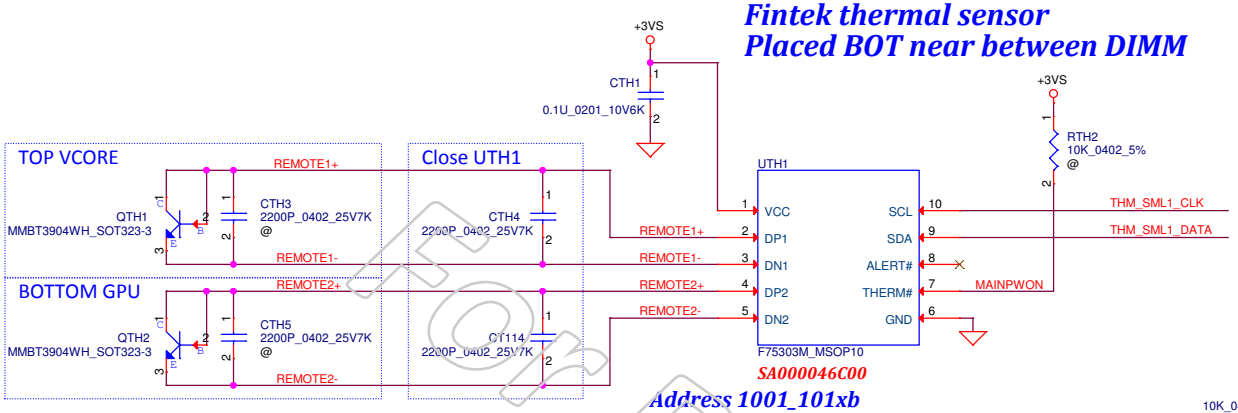
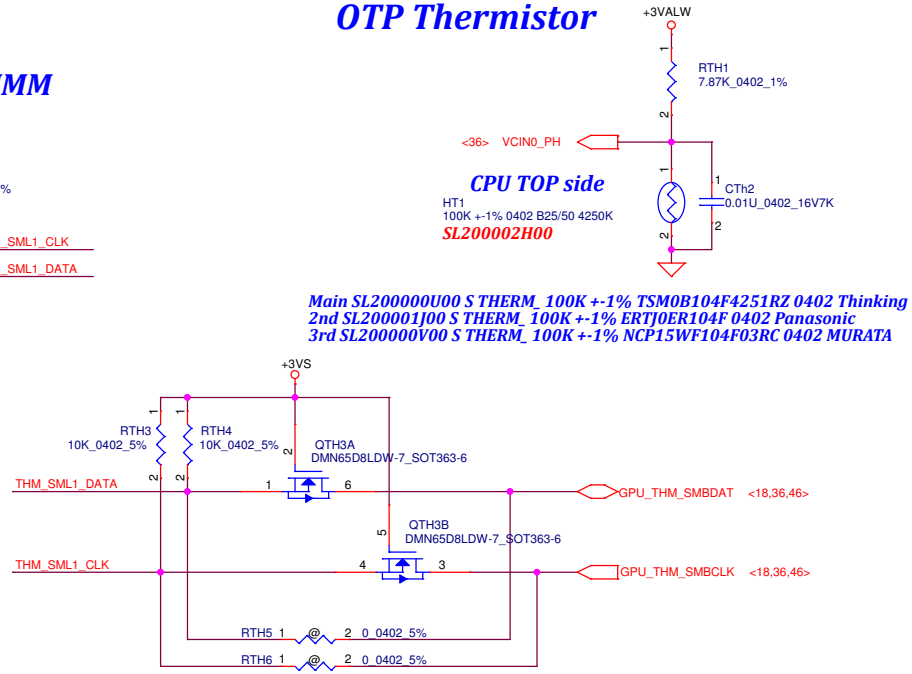
Thermal Sensor



OTP Thermistor



TPM

DVT1.0
Add RTPM5 BOM option for LA-E991P and LA-E992P EA difference.

RTPM5 991@TPM@
27_0402_5%
SD028270A80

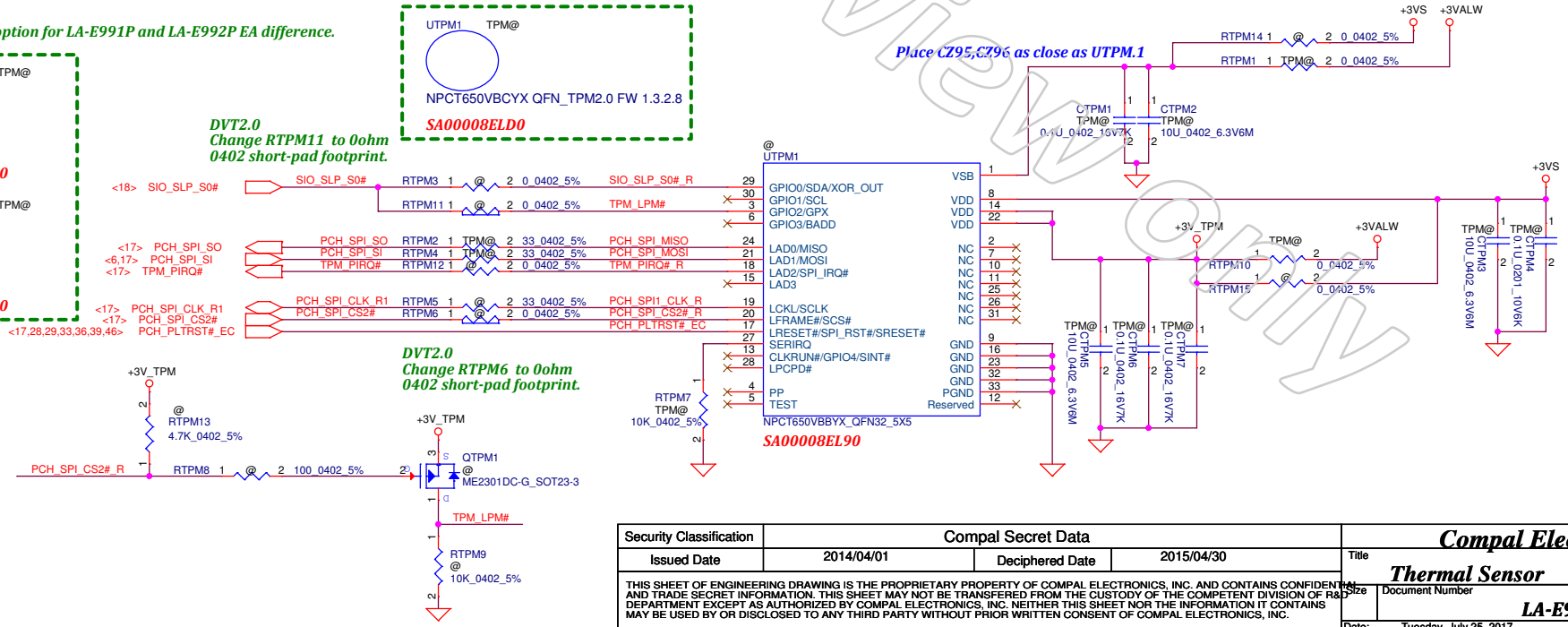
RTPM5 992@TPM@
33_0402_5%
SD028330A80

DVT1.0
Change TPM to NPCT650VBCYX with new FW version.

UTPM1 TPM@
NPCT650VBCYX QFN_TPM2.0 FW 1.3.2.8
SA00008ELD0

DVT2.0
Change RTPM11 to 0ohm
0402 short-pad footprint.

DVT2.0
Change RTPM6 to 0ohm
0402 short-pad footprint.



Security Classification	Compal Secret Data		
Issued Date	2014/04/01	Deciphered Date	2015/04/30

Compal Electronics, Inc.

Title: Thermal Sensor

Size | Document Number: LA-E992P | Rev: 1.0(A00)

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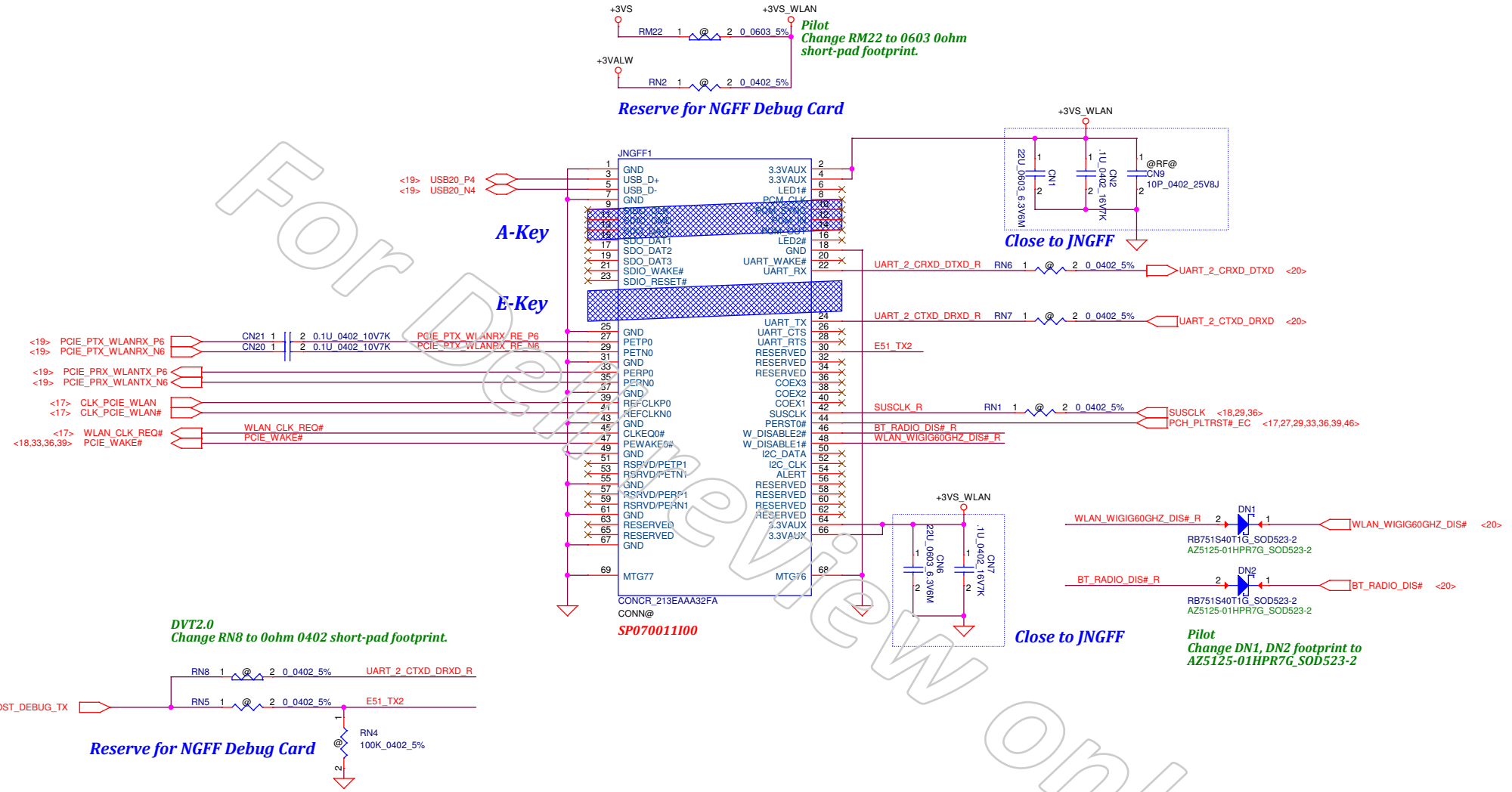
M.2 Key-E (WLAN + BT)



DVT2.0
Change RN8 to 0ohm 0402 short-pad footprint.

Key-E Debug Card Socket

	Standard NGFF pin define	Debug Card NGFF pin define
3.3VAUX	2, 4, 72, 74	2, 4, 56, 58
GND	1, 7, 18, 33, 39, 45, 51, 57, 63, 69, 75	1, 7, 10, 17, 23, 29, 35, 41, 47, 53, 59
NGFF_UART_TX	22	14
NGFF_UART_RX	32	16
EC_TX_P80DATA	38	22
EC_RX_P80CLK	40	24
PLT_RST#	52	36
NGFF_I2C_DATA	58	42
NGFF_I2C_CLK	60	44

Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: NGFF-WLAN

Size: Custom | Document Number: LA-E992P | Rev: 1.0(A00)

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M.2 Key-M (SSD)

PCIe SSD

SATA SSD

Pilot
Change RZ36 to 0805
0ohm short-pad footprint.

+3VS — RZ36 1 @ 2 0_0805_5% — +3.3VDX_SSD

JNGFF2

1	GND	3P3VAUX	2
3	GND	3P3VAUX	4
5	PERn3	NC	6
7	PERp3	NC	8
9	GND	DAS/DSS#	10
11	PETn3	3P3VAUX	12
13	PETp3	3P3VAUX	14
15	GND	3P3VAUX	16
17	PERn2	3P3VAUX	18
19	PERp2	NC	20
21	GND	NC	22
23	PETn2	NC	24
25	PETp2	NC	26
27	GND	NC	28
29	PERn1	NC	30
31	PERp1	NC	32
33	GND	NC	34
35	PETn1	NC	36
37	PETp1	DEVSLP	38
39	GND	NC	40
41	PERn0/SATA-B+	NC	42
43	PERp0/SATA-B-	NC	44
45	GND	NC	46
47	PETn0/SATA-A-	NC	48
49	PETp0/SATA-A+	NC	50
51	GND	PERST#	52
53	REFCLKN	CLKREQ#	54
55	REFCLKP	PEWake#	56
57	GND	NC	58
59	NC	SUSCLK(32kHz)	60
61	PEDET(NC-PCIE/GND-SATA)	3P3VAUX	62
63	GND	3P3VAUX	64
65	GND	3P3VAUX	66
67	GND	GND1	68
		GND2	69

BELLW_SD-80159-4221
CONN@
SP07001D300

PCIe signals:
- <16> PCIE_PRX_SSDTX_N12 / <16> PCIE_PRX_SSDTX_P12
- <16> PCIE_PTX_SSDRX_N12 / <16> PCIE_PTX_SSDRX_P12 — CD37 1 2 0.22U 0402 10V6K PCIE_PTX_SSDRX_N12_C; CD42 1 2 0.22U 0402 10V6K PCIE_PTX_SSDRX_P12_C
- <16> PCIE_PRX_SSDTX_N11 / <16> PCIE_PRX_SSDTX_P11
- <16> PCIE_PTX_SSDRX_N11 / <16> PCIE_PTX_SSDRX_P11 — CD43 1 2 0.22U 0402 10V6K PCIE_PTX_SSDRX_N11_C; CD44 1 2 0.22U 0402 10V6K PCIE_PTX_SSDRX_P11_C
- <16> PCIE_PRX_SSDTX_N10 / <16> PCIE_PRX_SSDTX_P10
- <16> PCIE_PTX_SSDRX_N10 / <16> PCIE_PTX_SSDRX_P10 — CD45 1 2 0.22U 0402 10V6K PCIE_PTX_SSDRX_N10_C; CD46 1 2 0.22U 0402 10V6K PCIE_PTX_SSDRX_P10_C

SATA signals:
- <16> SATA_PRX_SSDTX_P0A / <16> SATA_PRX_SSDTX_N0A
- <16> SATA_PTX_SSDRX_N0A / <16> SATA_PTX_SSDRX_P0A — CD53 1 2 0.22U 0402 10V6K SATA_PTX_SSDRX_N0A_C; CD51 1 2 0.22U 0402 10V6K SATA_PTX_SSDRX_P0A_C

<17> CLK_PCIE_SSD# / <17> CLK_PCIE_SSD

<16> mCARD_PCIE_SATA# — RD58 1 @ 2 0_0402_5%

DVT2.0
Change RD58 to 0ohm
0402 short-pad footprint.

SSD_LED# — SSD_LED# <37>

RF Reserved.
CD36 4.7U_0603_6.3V6K; CD37 0.1U_0402_10V6K; CD38 0.01U_0402_16V7K; CD39 47P_0402_50V8J; CD40 15P_0402_50V8J; CD41 RF@

DVT1.0
Un-pop RD7

RD7 2 @ 1 10K_0402_5% — +3.3VDX_SSD

RD59 1 @ 2 0_0402_5% — mSATA_DEVSLP <19>

DVT2.0
Change RD59 to 0ohm 0402 short-pad footprint.

PCH_PLTRST#_EC <17,27,28,33,36,39,46>
SSD_CLK_REQ# <17>
SSD_PCIE_WAKE# — RD8 1 2 10K_0402_5% — +3.3VDX_SSD

RD9 1 @ 2 0_0402_5% — SUSCLK <18,28,36>

Free Fall Sensor

+3VS — CN19 FFS@ 0.1U_0402_16V7K; CN22 @ 10U_0603_6.3V6M

U5603 FFS@ LNG2DM

10	VDD_IO	RES	5
9	VDD		
		INT 1	12
		INT 2	11
3	SDO/SA0		
4	SDA/SDI/SDO		
1	SCL/SPC		
		GND	6
		GND	7
		GND	8
2	CS		

LNG2DMTR_LGA12_2X2
SA000089W00

<6,14,15,18,35> PCH_SMBDATA
<6,14,15,18,35> PCH_SMBCLK

+3VS — RS40 100K_0402_5%; RS41 100K_0402_5% — FFS_INT1 / FFS_INT2 — FFS_INT1 <20> / FFS_INT2 <17>

+5VS_HDD — FFS@ RS1 100K_0402_5% — FFS_INT2_Q

+3VS — FFS@ RS39 100K_0402_5%

FFS@ QC5A DMN65D8LDW-7_SOT363-6

FFS@ QC5B DMN65D8LDW-7_SOT363-6

FFS_INT2

HDD CONN

Pilot
Change RZ34 to 0805
0ohm short-pad footprint.

+5VS — RZ34 1 @ 2 0_0805_5% — +5VS_HDD

DVT2.0
Change JHDD1 to ACES_51625-01201-001

JHDD1

<16> SATA_PTX_DRX_P1B	CS28	SATA_PTX_DRX_P1B_RC	1
<16> SATA_PTX_DRX_N1B	CS27	SATA_PTX_DRX_N1B_RC	2
			3
			4
<16> SATA_PRX_DTX_N1B	CS25	SATA_PRX_DTX_N1B_RC	5
<16> SATA_PRX_DTX_P1B	CS26	SATA_PRX_DTX_P1B_RC	6
			7
<19> HDD_DEVSLP	RD62	HDD_DEVSLP_R	8
		FFS_INT2_Q	9
+5VS_HDD			10
			11
			12
		GND	13
		GND	14

CONN@
ACES_51625-01201-001
SP010028W00

Place near HDD CONN (JHDD1)

+5VS_HDD — CS12 1000P_0402_50V7K; CS13 0.1U_0402_10V6K; CS14 1U_0402_6.3V6K; CS15 10U_0603_6.3V6M

Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: SSD/HDD

Size: Custom | Document Number: LA-E992P | Rev: 1.0(A00)

Date: Tuesday, July 25, 2017 | Sheet 29 of 77

Reserved

Security Classification	Compal Secret Data		
Issued Date	2013/07/04	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **Reserved**

Size | Document Number: **LA-E992P** | Rev: 1.0(A00)

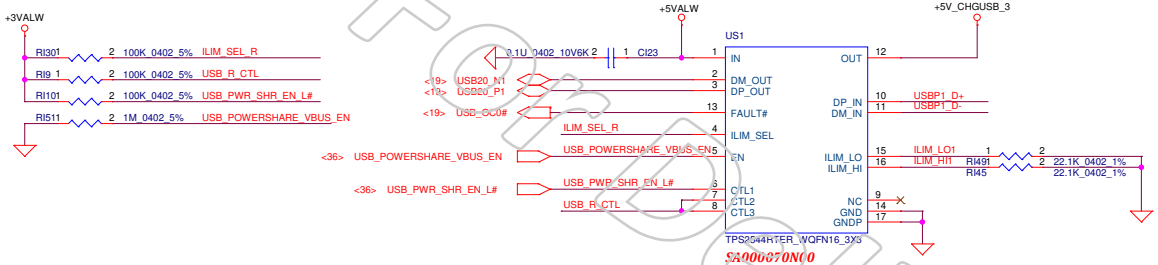
Date: Tuesday, July 25, 2017 | Sheet 30 of 77

USB Powershare

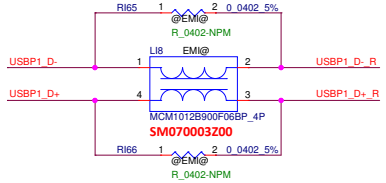
Device Control Pins				Flow Line Condition
CTL1	CTL2	CTL3	ILIM_SEL	
0	1	1	X	DCP AUTO
1	1	1	0	SDP
1	1	1	1	CDP

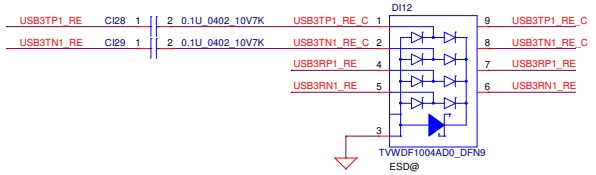
Suspend mode	CTL1 = 0 : Enable Power Share DCP mode in Suspend mode
	CTL1 = 1 : Disable Power Share in Suspend mode (For Support USB wake)
S0 mode	ILIM_SEL = 0 : SDP mode (0.9A by ILIM_LO setting)
	ILIM_SEL = 1 : CDP mode (STATUS# trigger by ILIM_HI =2.2A)

USB3.0 / USB2.0 Port1



Pilot
Change RI65, RI66 footprint to R_0402-NPM





Place close to JUSB3

USB3.0 Re-driver

Setting Status

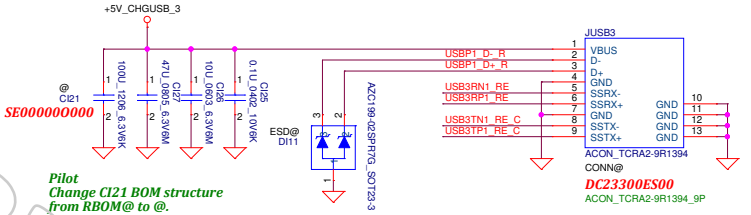
	B_EQ		A_EQ		B_DE		A_DE	
PI3EQX7502AI	NC	6.0dB	NC	6.0dB	NC	-3.5dB	NC	-3.5dB
	0	3.0dB	0	3.0dB	0	0.0dB	0	0.0dB
	1	9dB	1	9dB	1	-6.0dB	1	-6.0dB
PS8713	A EQ0 EQ1	A_EQ	B EQ0 EQ1	B_EQ	A DE0 DE1	A_DE	B DE0 DE1	B_DE
	0 0	9.5dB	0 0	9.5dB	0 0	-3.5dB	0 0	-3.5dB
	0 1	4.5dB	0 1	4.5dB	0 1	-2.7dB	0 1	-2.7dB
	1 0	13 dB	1 0	13 dB	1 0	0.0dB	1 0	0.0dB
	1 1	7.5dB	1 1	7.5dB	1 1	-5.0dB	1 1	-5.0dB

* red color is current setting

From PCH
PERICOM: RXA, PS8713: B_In
PERICOM: TXB, PS8713: A_Out

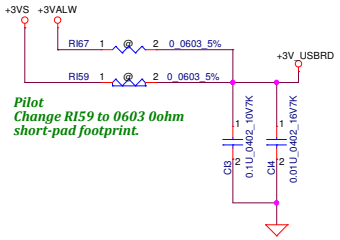
To USB3 CONN
PERICOM: TXA, PS8713:B_Out
PERICOM: RXB, PS8713:A_In

USB3.0 / USB2.0 Left Side

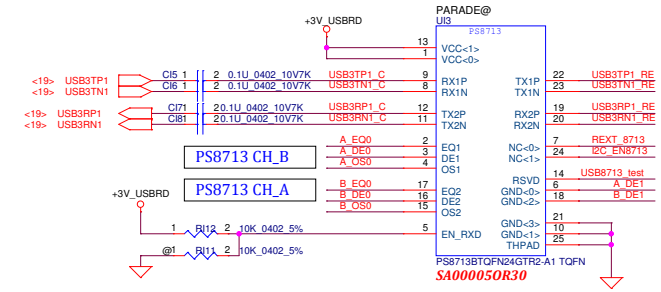


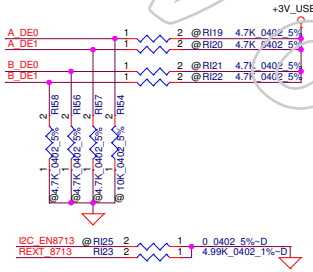
Pilot
Change CI21 BOM structure
from RBOM@ to @.

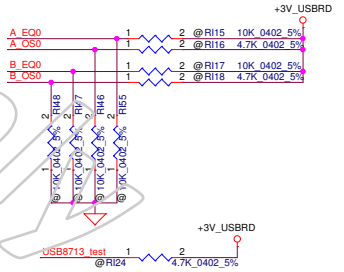
Pilot
Change JUSB3 footprint from
SINGA_2UB2309-000111F_9P-T to
ACON_TCRA2-9R1394_9P



Pilot
Change RI59 to 0603 0ohm
short-pad footprint.







DVT2.0
Remove UI3 TI@ BOM option

PS8713:
Pin8,9=B_In, P22,23=B_Out
Pin11,12=A_Out, Pin19,20=A_In
Pin 17=A_EQ0, Pin 15=A_EQ1
Pin 16=A_DE0, Pin 18=A_DE1
Pin 2=B_EQ0, Pin 4=B_EQ1
Pin 3=B_DE0, Pin 6=B_DE1

UI3 PERICOM@
PI3EQX7502AIZDEX TQFN24 USB3.0 REDR
SA00006WV00

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/08/25	Deciphered Date 2012/07/25	Title: USB Powershare
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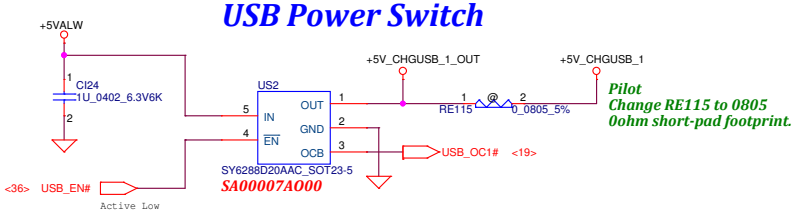
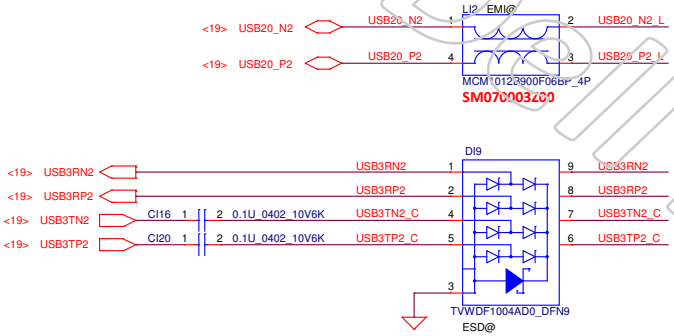
USB Power Switch



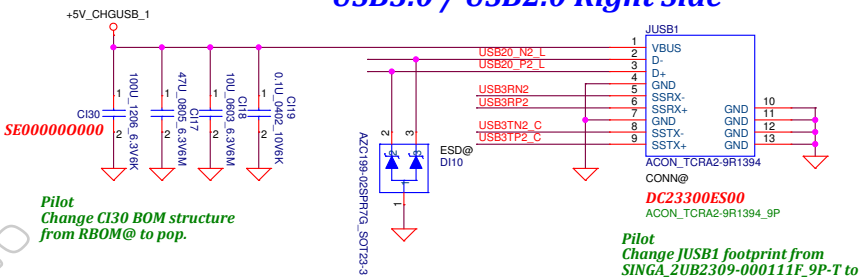
Pilot
Change RE115 to 0805
0ohm short-pad footprint.

+5VALW
+5V_CHGUSB_1
+5V_CHGUSB_1_OUT
Trace width : 100mil



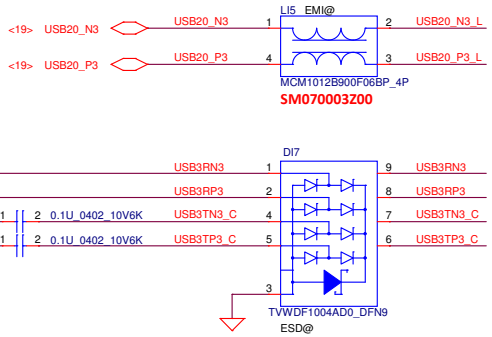
Place close to JUSB1

USB3.0 / USB2.0 Right Side



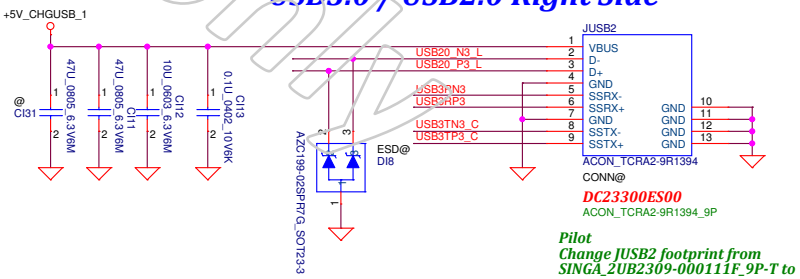
Pilot
Change CI30 BOM structure
from RBOM@ to pop.

Pilot
Change JUSB1 footprint from
SINGA_2UB2309-000111F_9P-T to
ACON_TCRA2-9R1394_9P



Place close to JUSB2

USB3.0 / USB2.0 Right Side



Pilot
Change JUSB2 footprint from
SINGA_2UB2309-000111F_9P-T to
ACON_TCRA2-9R1394_9P

Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: **USB conn.**

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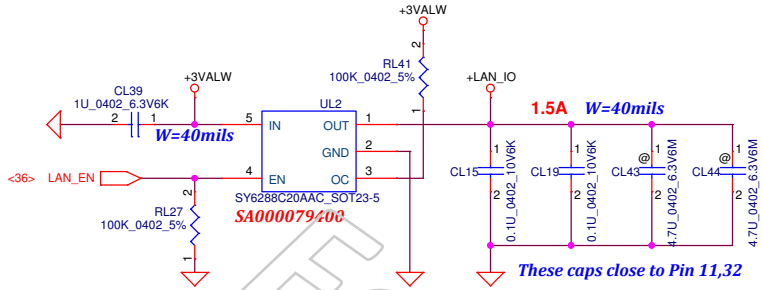
LOM + RJ45

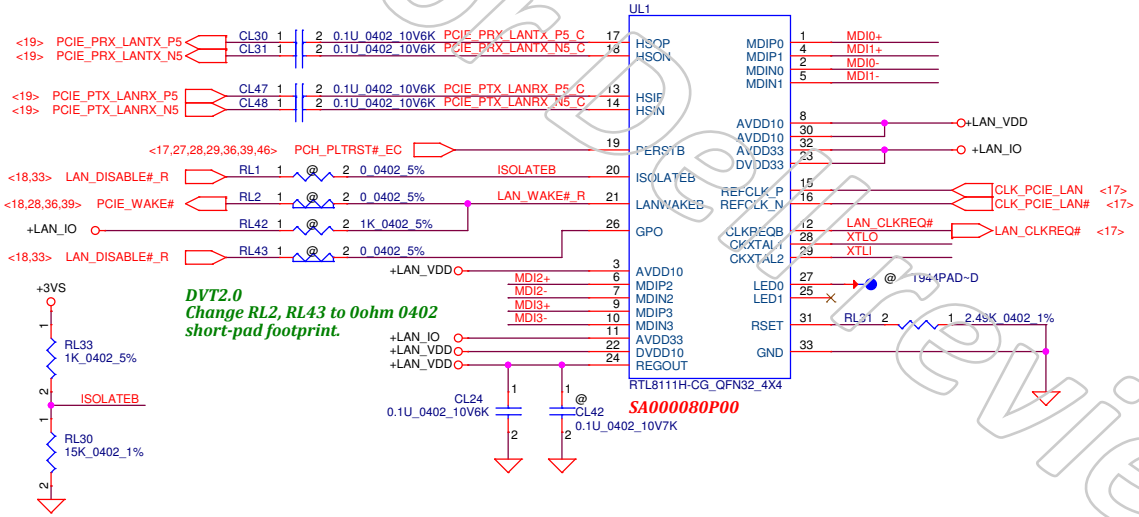
+LAN_IO rising time : >1ms and <100ms



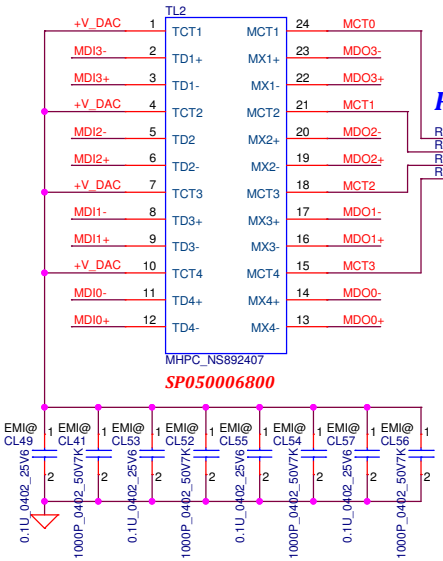
DVT2.0
Remove DL1, DL2

Main SP050006800 S X'FORM_ NS892407 1G MHPC
2nd SP050006B10 S X'FORM_ GST5009-E LF LAN BOTHHAND
3rd SP050006F00 S X'FORM_ IH-160 LAN TAIMAG

DVT2.0
Change SP050006800 as main source.

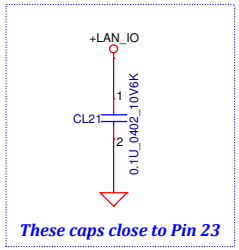


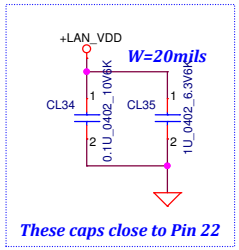
DVT2.0
Change RL2, RL43 to 0ohm 0402
short-pad footprint.

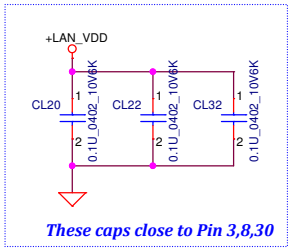


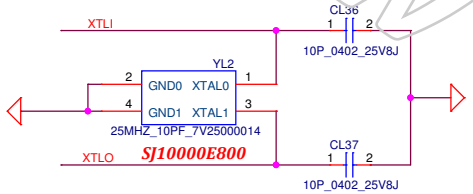
Place close to MCT pin

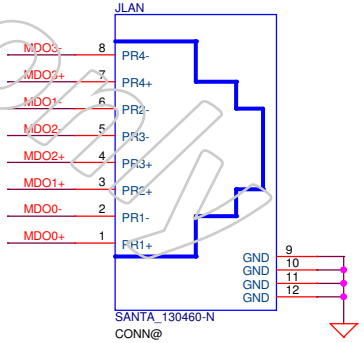
DVT2.0
Remove SP050009200
BOM option.











6.8. GPO Pin

Table 8. GPO Pin

Symbol	Type	Pin No	Description
GPO/LED1	I/O	26	General Purpose Input/Output Pin (1.8V/3.3V compatible input, 3.3V output only). The setting is changed from the register. Only one function (LED1 or GPIO) may be selected at one time (default: LED1). Power Saving Feature: Output pin. Link OK Feature: Output pin. PHY Disable Mode (active low): Input pin.

Note: The LED1 pin can be changed to a GPO pin. The setting is changed from the register. Only one function (LED1 or GPIO) may be selected at one time (Default: LED1).

Security Classification	Compal Secret Data		
Issued Date	2013/08/01	Deciphered Date	2014/07/31

Compal Electronics, Inc.

Title: **LAN RTL8111GUS-CG**

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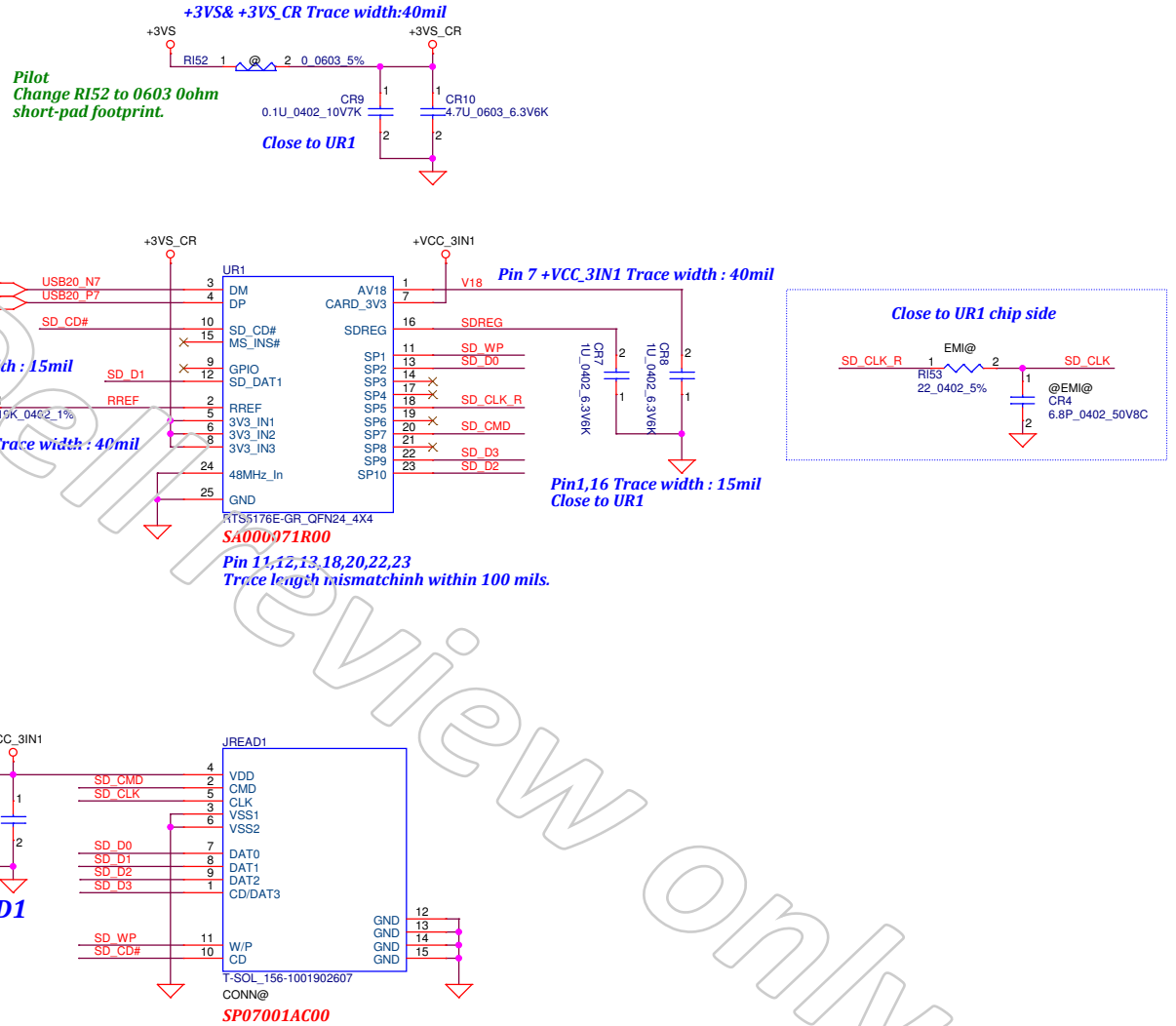
Card Reader



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2015/09/01	Deciphered Date	2016/09/01
Title: Crad Reader RTS5176E			
Size	Document Number: LA-E992P		Rev: 1.0(A00)
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Main Func = DP to VGA Converter

+3VS RVGA1 1 @ 2 0_0603_5% AVCC33
Pilot
Change RVGA1 to 0603
0ohm short-pad footprint.
CVGA1 10U_0603_6.3V6M VGA@

+3VS RVGA2 1 @ 2 0_0603_5% VDD_DAC_33
Pilot
Change RVGA2 to 0603
0ohm short-pad footprint.
CVGA2 10U_0603_6.3V6M VGA@

+CRT_5V_OUT FVGA1 1.1A_6V_SPR-P110 VGA@ DVGA1 LRB551V-30T1G_SOD323-2 VGA@ +5VS

+3VS
DDI3_AUXN_C RVGA3 100K_0402_5%
DDI3_AUXP_C RVGA4 100K_0402_5%

Note:
CG3, CG4. CG6, CG8, CG15 need to place to Chip

UVGA1 RTD2166 RTD2166-CG_QFN32_4X4

AVCC33	1	VDD_DAC_33	20
AVCC_12	4	VCCK_12	25
VCC_33	14	PVCC_33	26
AUX_P	2	HVSYNC_PWR	17
AUX_N	3	VSYNC	18
LANE0_P	5	HSYNC	19
LANE0_N	6	BLUE_P	21
LANE1_P	7	GREEN_P	22
LANE1_N	8	RED_P	23
POL1/SPI_CEB	10	LDO_RSTB	27
POL2	9	EXT_CLK_IN	28
GPI1/SPI_CLK	11	EXT1.2V_CTRL	31
GPI2/SPI_SI	12	GND	24
GPI3/SPI_SO	13	EPAD_GND	33
VGA_SCL	15		
VGA_SDA	16		
SMB_SCL	30		
SMB_SDA	29		
HPD	32		

CVGA6 VGA@1 2 0.1U_0402_16V4Z +1.2V_VCCK
+3VS
<7> DDI3_AUXP DDI3_AUXP CVGA4 VGA@1 2 0.1U_0402_16V4Z DDI3_AUXP_C
<7> DDI3_AUXN DDI3_AUXN CVGA9 VGA@1 2 0.1U_0402_16V4Z DDI3_AUXN_C
<7> CPU_DDI3_P0 CPU_DDI3_P0 CVGA10 VGA@1 2 0.1U_0402_16V4Z DP_P0
<7> CPU_DDI3_N0 CPU_DDI3_N0 CVGA11 VGA@1 2 0.1U_0402_16V4Z DP_N0
<7> CPU_DDI3_P1 CPU_DDI3_P1 CVGA12 VGA@1 2 0.1U_0402_16V4Z DP_P1
<7> CPU_DDI3_N1 CPU_DDI3_N1 CVGA13 VGA@1 2 0.1U_0402_16V4Z DP_N1
AVCC33 RVGA5 VGA@2 1 4.7K_0402_5% POL1_SDA
RVGA6 VGA@2 1 4.7K_0402_5% POL1_SCL
+3VS RVGA16 @ 1 4.7K_0402_5%
CRT_DDCCLK_CON
CRT_DDCDATA_CON
<6,14,15,18,29> PCH_SMBCLK
<6,14,15,18,29> PCH_SMBDATA
<16> CPU_DDI3HPD CPU_DDI3HPD RVGA9 1 @ 2 0_0402_5% CRT_PCH_HPD

DVT2.0
Change RVGA9 to 0ohm 0402
short-pad footprint.

RVGA10 100K_0402_5%

+CRT_5V_OUT
RVGA7 2.2K_0402_5% VGA@
RVGA8 2.2K_0402_5% VGA@
CRT_DDCDATA_CON
CRT_DDCCLK_CON

VDD_DAC_33
CVGA3 VGA@1 2 0.1U_0402_16V4Z
CVGA5 VGA@1 2 2.2U_0402_6.3V6M
+1.2V_VCCK CVGA7 VGA@1 2 0.1U_0402_16V4Z
+3VS CVGA8 VGA@1 2 0.1U_0402_16V4Z
+5VS
DP_CRT_VSYNC_CON
DP_CRT_HSYNC_CON
DP_CRT_B
DP_CRT_G
DP_CRT_R
4.7U_0603_6.3V6K CVGA14 VGA@
0.1U_0402_16V4Z CVGA15 VGA@

CRT RGB
CRT H/VSYNC
CRT SMBUS

DVT 1.0
Change LVGA1, LVGA2, LVGA3 BS to VGA@EMI@.

DP_CRT_R LVGA11 VGA@EMI@ BLM15BB220SN1D CRT_R
DP_CRT_G LVGA21 VGA@EMI@ BLM15BB220SN1D CRT_G
DP_CRT_B LVGA31 VGA@EMI@ BLM15BB220SN1D CRT_B
RVGA11 RVGA12 RVGA13 75_0402_1%
CVGA16 CVGA17 CVGA18 CVGA19 CVGA20 CVGA21 2.2P_0402_50V8C

+CRT_5V_OUT JCRT1
CRT_R
CRT_DDCDATA_CON
CRT_G
CRT_HSYNC_CON
CRT_B
CRT_VSYNC_CON
CRT_DDCCLK_CON
CVGA22 0.01U_0402_16V7K
C-K_80454-5K1-152 CONN@
DC060004S10

1. Red Video
2. Green Video
3. Blue Video
4. No Connect
5. Ground
6. Red Return
11. No Connect
7. Green Return
12. DDC Data
8. Blue Return
13. Horizontal Sync
9. DDC Power
14. Vertical Sync
10. Sync Return
15. DDC Clock

DP_CRT_HSYNC_CON 47_0402_5% RVGA14 CRT_HSYNC_CON
DP_CRT_VSYNC_CON 47_0402_5% RVGA15 CRT_VSYNC_CON
CVGA23 10P_0402_50V VGA@EMI@
CVGA24 10P_0402_50V VGA@EMI@

DVT 1.0
Change CVGA23, CVGA24 BS to VGA@EMI@.

Security Classification	Compal Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/09/01

Compal Electronics, Inc.

Title: **DP to VGA Converter**

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Custom	LA-E992P	1.0(A00)

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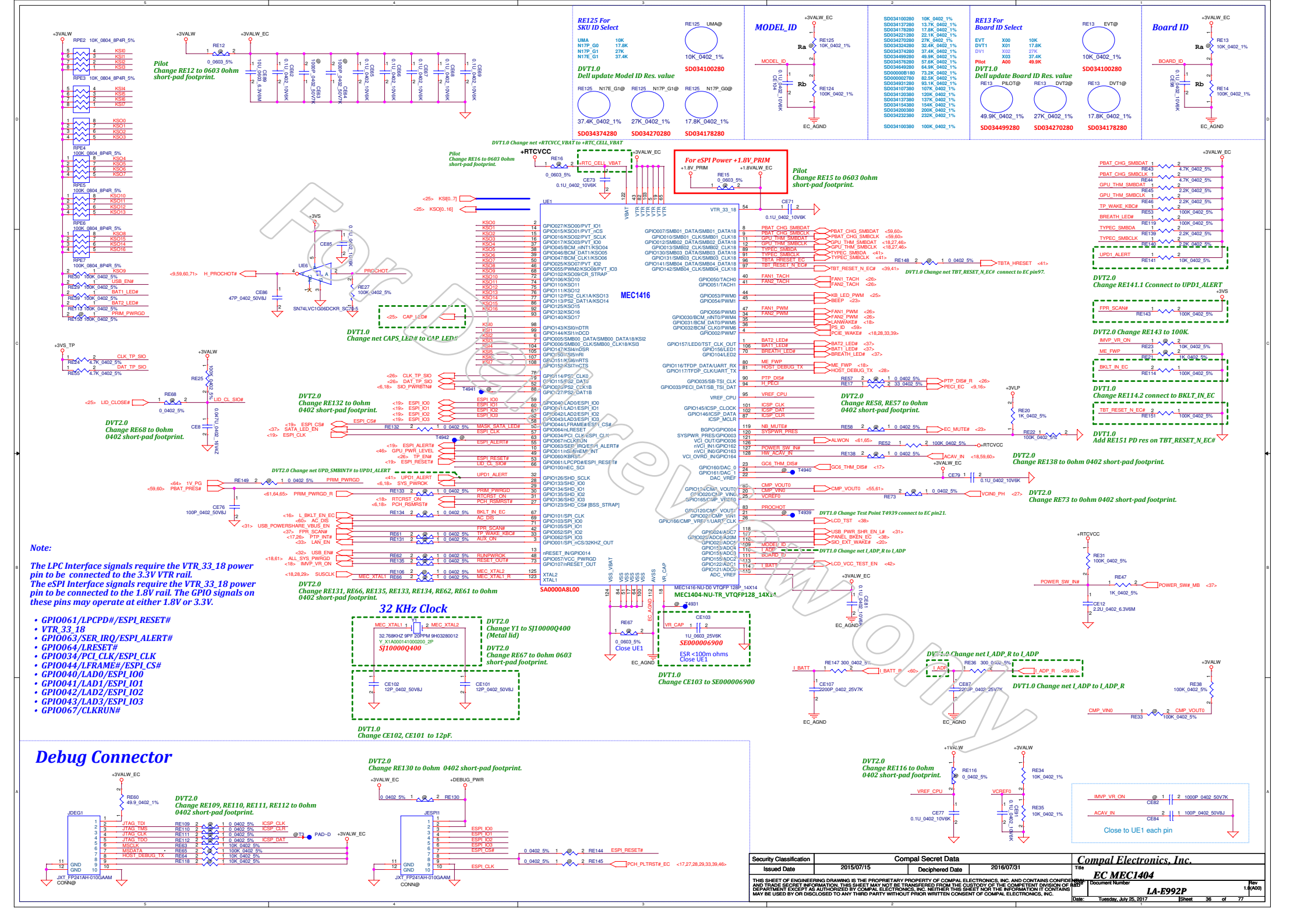
RE125 For SKU ID Select
UMA 10K
N17P_G0 17.8K
N17P_G1 27K
N17E_G1 37.4K
RE125 UMA@
10K_0402_1%
SD034100280
DVT1.0 Dell update Model ID Res. value
RE125_N17E_G1@ 37.4K_0402_1%
SD034374280
RE125_N17P_G1@ 27K_0402_1%
SD034270280
RE125_N17P_G0@ 17.8K_0402_1%
SD034178280
MODEL_ID
RE125 10K_0402_1%
RE124 100K_0402_1%
EC_AGND
SD034100280 10K_0402_1%
SD034137380 13.7K_0402_1%
SD034178280 17.8K_0402_1%
SD034221280 22.1K_0402_1%
SD034270280 27K_0402_1%
SD034324280 32.4K_0402_1%
SD034374280 37.4K_0402_1%
SD034498280 49.9K_0402_1%
SD034576280 57.6K_0402_1%
SD034649280 64.9K_0402_1%
SD000008180 73.2K_0402_1%
SD000002780 82.5K_0402_1%
SD034931280 93.1K_0402_1%
SD034107380 107K_0402_1%
SD034120380 120K_0402_1%
SD034137380 137K_0402_1%
SD034154380 154K_0402_1%
SD034200380 200K_0402_1%
SD034232380 232K_0402_1%
SD034100380 100K_0402_1%
RE13 For Board ID Select
EVT X00 10K
DVT1 X01 17.8K
DV1 X02 27K
X03 37.4K
Pilot A00 49.9K
RE13 EVT@
10K_0402_1%
SD034100280
DVT1.0 Dell update Board ID Res. value
RE13 PILOT@ 49.9K_0402_1%
SD034499280
RE13 DVT2@ 27K_0402_1%
SD034270280
RE13 DVT1@ 17.8K_0402_1%
SD034178280
Board ID
BOARD_ID
RE13 10K_0402_1%
RE14 100K_0402_1%
EC_AGND
Pilot Change RE12 to 0603 0ohm short-pad footprint.
DVT1.0 Change net +RTCVCC_VBAT to +RTC_CELL_VBAT
Pilot Change RE16 to 0603 0ohm short-pad footprint.
For eSPI Power +1.8V_PRIM
Pilot Change RE15 to 0603 0ohm short-pad footprint.
MEC1416
MEC1416-NU-D0 VTQFP 128P_14X14
MEC1404-NU-TR_VTQFP128_14X14
SA0000A8L00
DVT1.0 Change net TBT_RESET_N_EC# connect to EC pin97.
DVT2.0 Change RE141.1 Cconnect to UPD1_ALERT
DVT2.0 Change RE143 to 100K.
DVT1.0 Change RE114.2 connect to BKLT_IN_EC
DVT1.0 Add RE151 PD res on TBT_RESET_N_EC#
DVT1.0 Change net CAPS_LED# to CAP_LED#
DVT2.0 Change RE132 to 0ohm 0402 short-pad footprint.
DVT2.0 Change RE68 to 0ohm 0402 short-pad footprint.
DVT2.0 Change net UPD_SMBINT# to UPD1_ALERT
DVT2.0 Change RE58, RE57 to 0ohm 0402 short-pad footprint.
DVT2.0 Change RE138 to 0ohm 0402 short-pad footprint.
DVT2.0 Change RE73 to 0ohm 0402 short-pad footprint.
DVT1.0 Change Test Point T4939 connect to EC pin21.
DVT2.0 Change RE131, RE66, RE135, RE133, RE134, RE62, RE61 to 0ohm 0402 short-pad footprint.
32 KHz Clock
DVT2.0 Change Y1 to SJ10000Q400 (Metal lid)
DVT2.0 Change RE67 to 0ohm 0603 short-pad footprint.
DVT1.0 Change CE103 to SE000006900
DVT1.0 Change net I_ADP_R to I_ADP
DVT1.0 Change CE102, CE101 to 12pF.
DVT2.0 Change RE130 to 0ohm 0402 short-pad footprint.
DVT2.0 Change RE116 to 0ohm 0402 short-pad footprint.
Note:
The LPC Interface signals require the VTR_33_18 power pin to be connected to the 3.3V VTR rail.
The eSPI Interface signals require the VTR_33_18 power pin to be connected to the 1.8V rail. The GPIO signals on these pins may operate at either 1.8V or 3.3V.
GPIO061/LPCPD#/ESPI_RESET#
VTR_33_18
GPIO063/SER_IRQ/ESPI_ALERT#
GPIO064/LRESET#
GPIO034/PCI_CLK/ESPI_CLK
GPIO044/LFRAME#/ESPI_CS#
GPIO040/LAD0/ESPI_IO0
GPIO041/LAD1/ESPI_IO1
GPIO042/LAD2/ESPI_IO2
GPIO043/LAD3/ESPI_IO3
GPIO067/CLKRUN#
Debug Connector
JDEG1
JESPI1
JXT_FP24AH-010GAAM
CONN@
Close to UE1 each pin
Security Classification Compal Secret Data
Issued Date 2015/07/15
Deciphered Date 2016/07/31
Compal Electronics, Inc.
EC MEC1404
Document Number LA-E992P
Rev 1.0(A00)
Date: Tuesday, July 25, 2017
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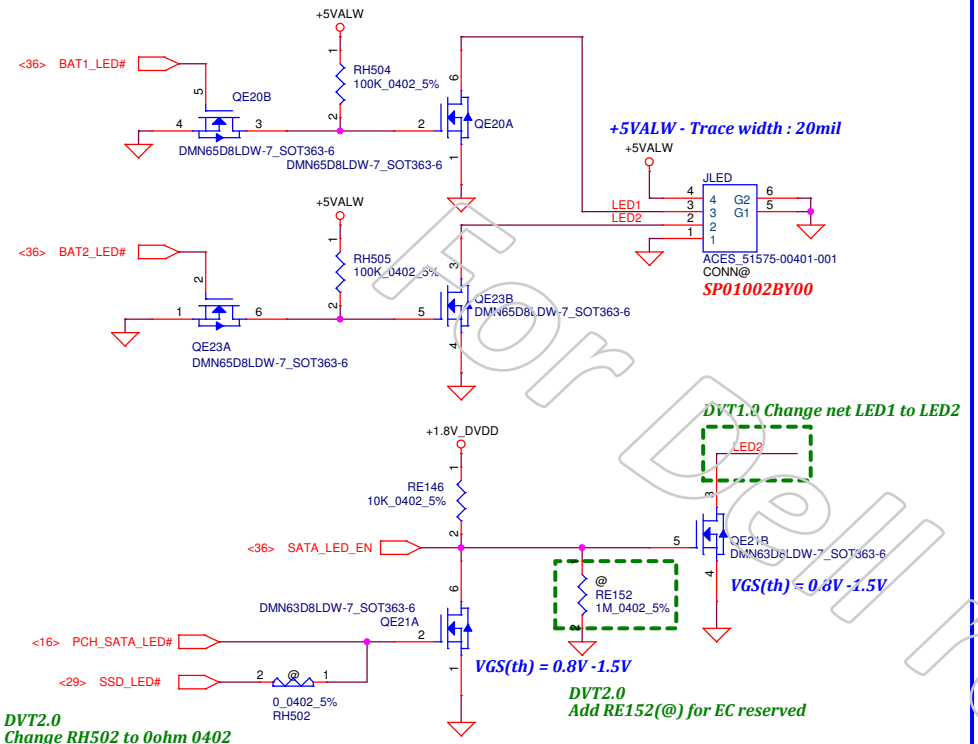
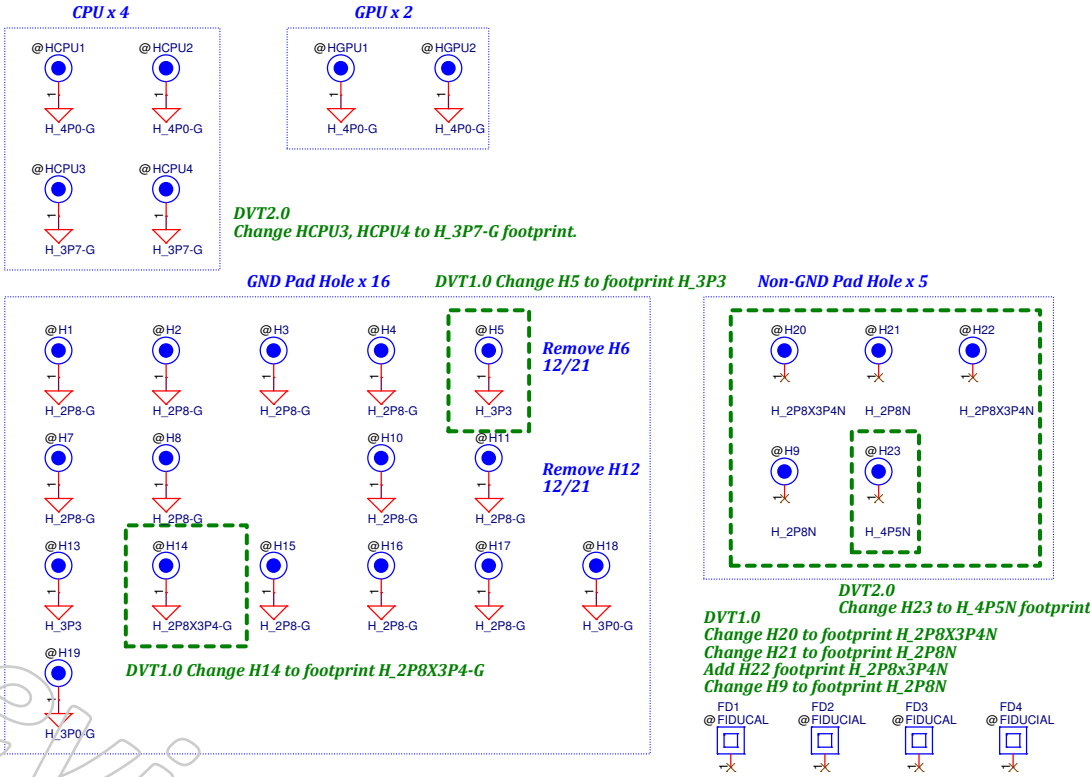
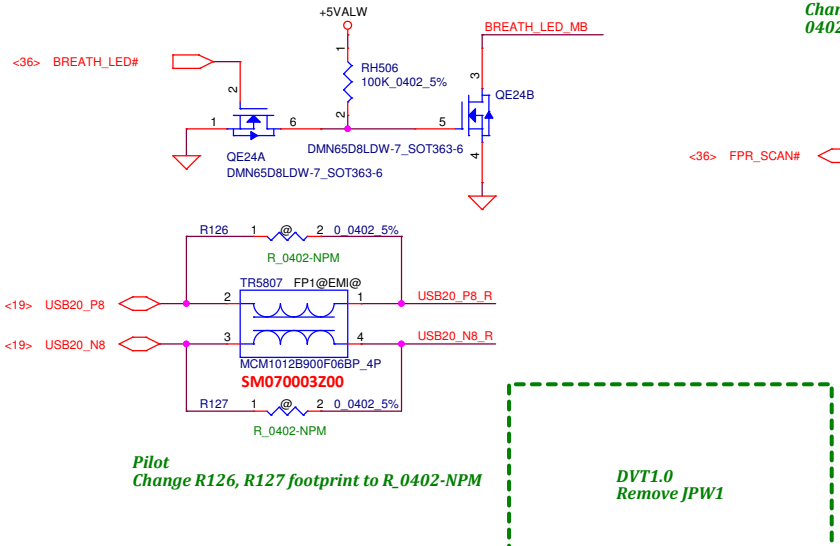
LED Board Connector



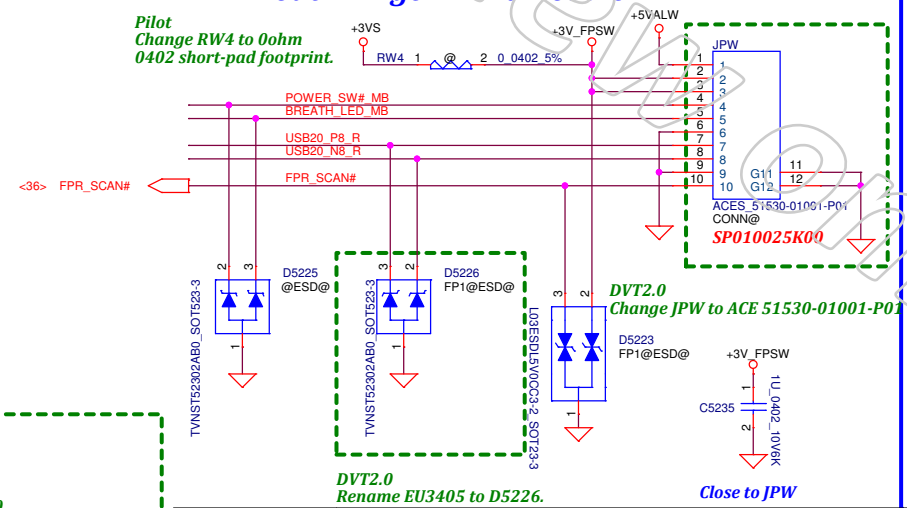
Screw Hole



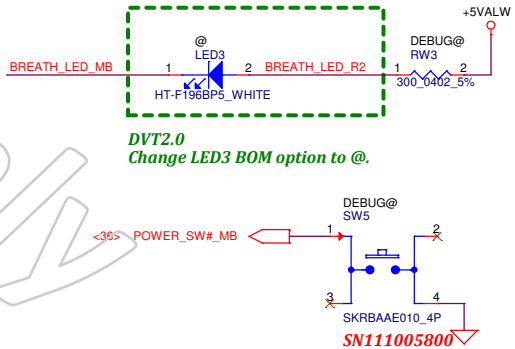
PWR BOARD Connector



Touch Finger Print module.



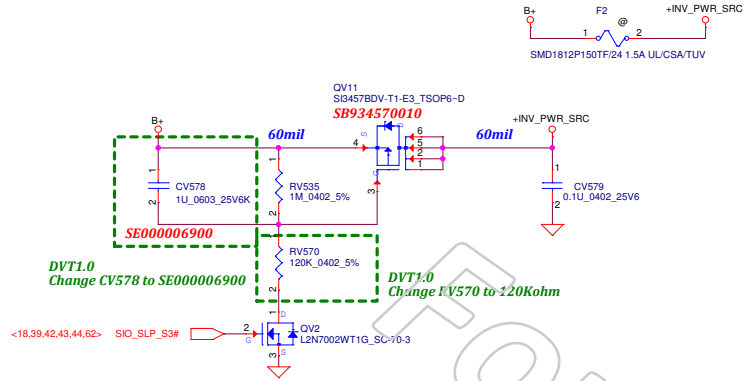
Power Button & LED (Reserve)



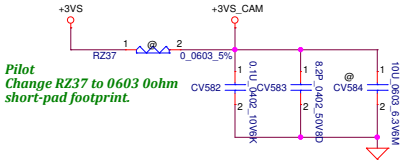
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

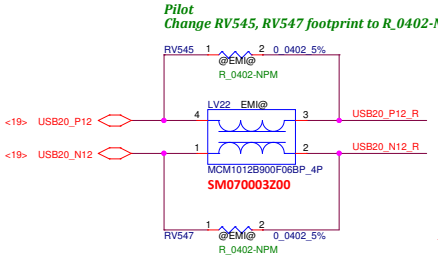
Compal Electronics, Inc.			
Title: TPM/BTB conn.			
Size	Document Number: LA-E992P		Rev: 1.0(A00)
Date: Tuesday, July 25, 2017	Sheet 37 of 77		

LCD backlight PWR CTRL



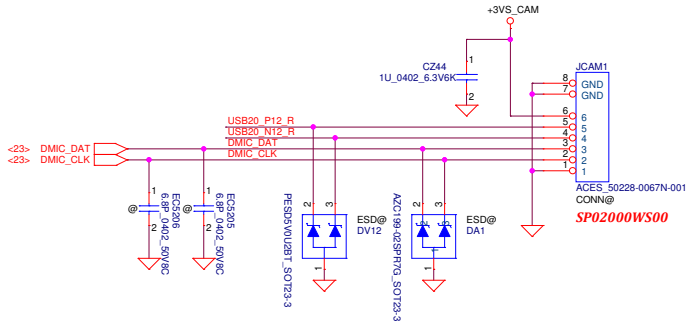
CCD +DMIC Circuit



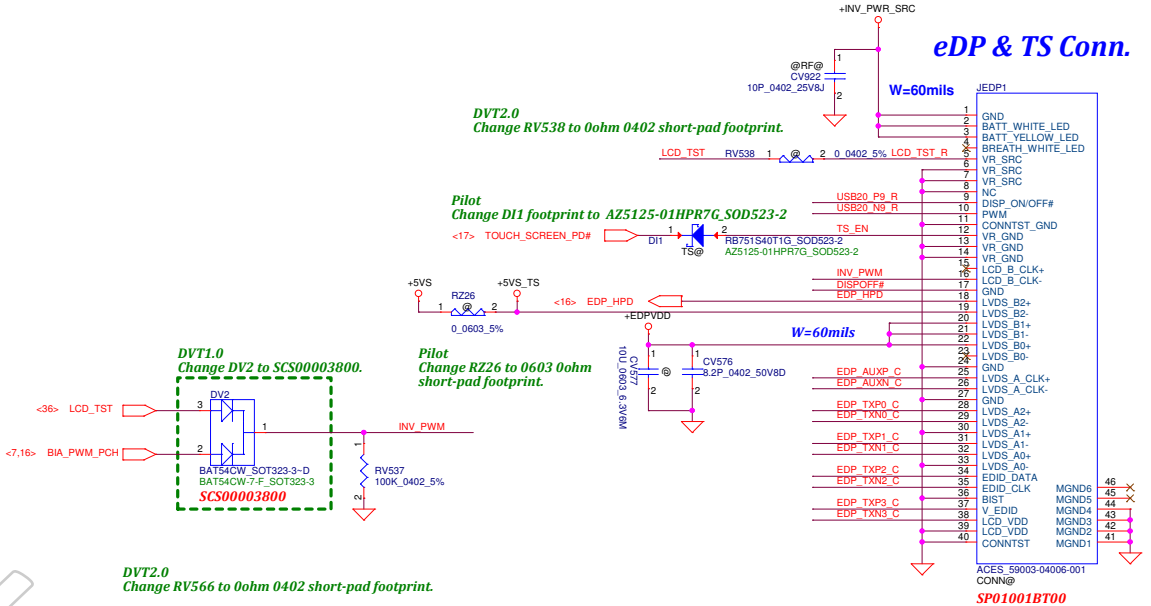


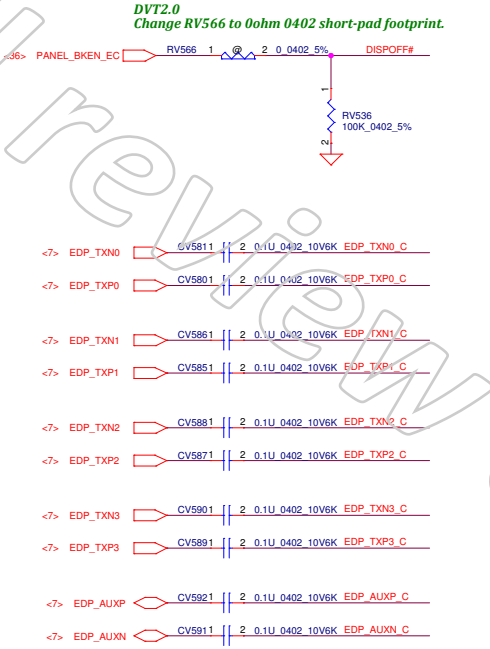
Need to check pin define

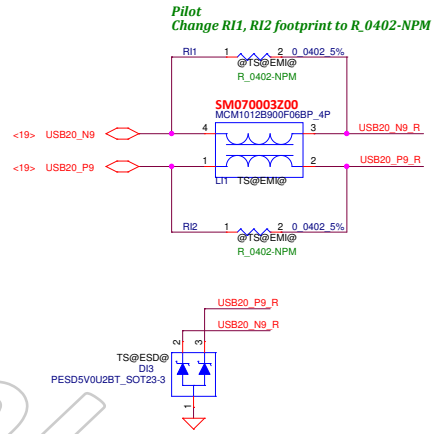
CCD +DMIC Connector



eDP & TS Conn.







Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/08/25	Deciphered Date 2012/07/25	Title: eDP /TS conn.
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			Date: Tuesday, July 25, 2017 Sheet 38 of 77

UT1 TBT@

S IC JHL6340 SLLSP C1 THUNDERBOLT A31!
SA00009YL3L

PCIE X4 Bus

PCIE CLK

DVT2.0
Change RT2 to 0 ohm
0201 short-pad footprint.

CPU DDI1

CPU DDI2

Reserve for common DP design

DVT1.0
Remove JTAG

UT1A

PCIe GEN3

SINK PORT 0

SOURCE PORT 0

SINK PORT 1

LC GPIO

POC GPIO

Misc

MISC

TBT PORTS

Port A

PORT B

POC

DEBUG

ALPINE-RIDGE_BGA337

DVT1.0 Un-pop RT30

Closed to UT1

DVT1.0 Un-pop RT80

DVT2.0 Change RT13, RT16 to 0 ohm
0201 short-pad footprint.

DVT2.0 Change RT121 to 0 ohm
0201 short-pad footprint.

SJ10000TZ00

DVT1.0
Remove RT98, RT99, RT100

DVT1.0
Remove Off- page connector

Close to UT1

DVT2.0
Change RT110 to 0 ohm 0201 short-pad footprint.

SA00003EW10

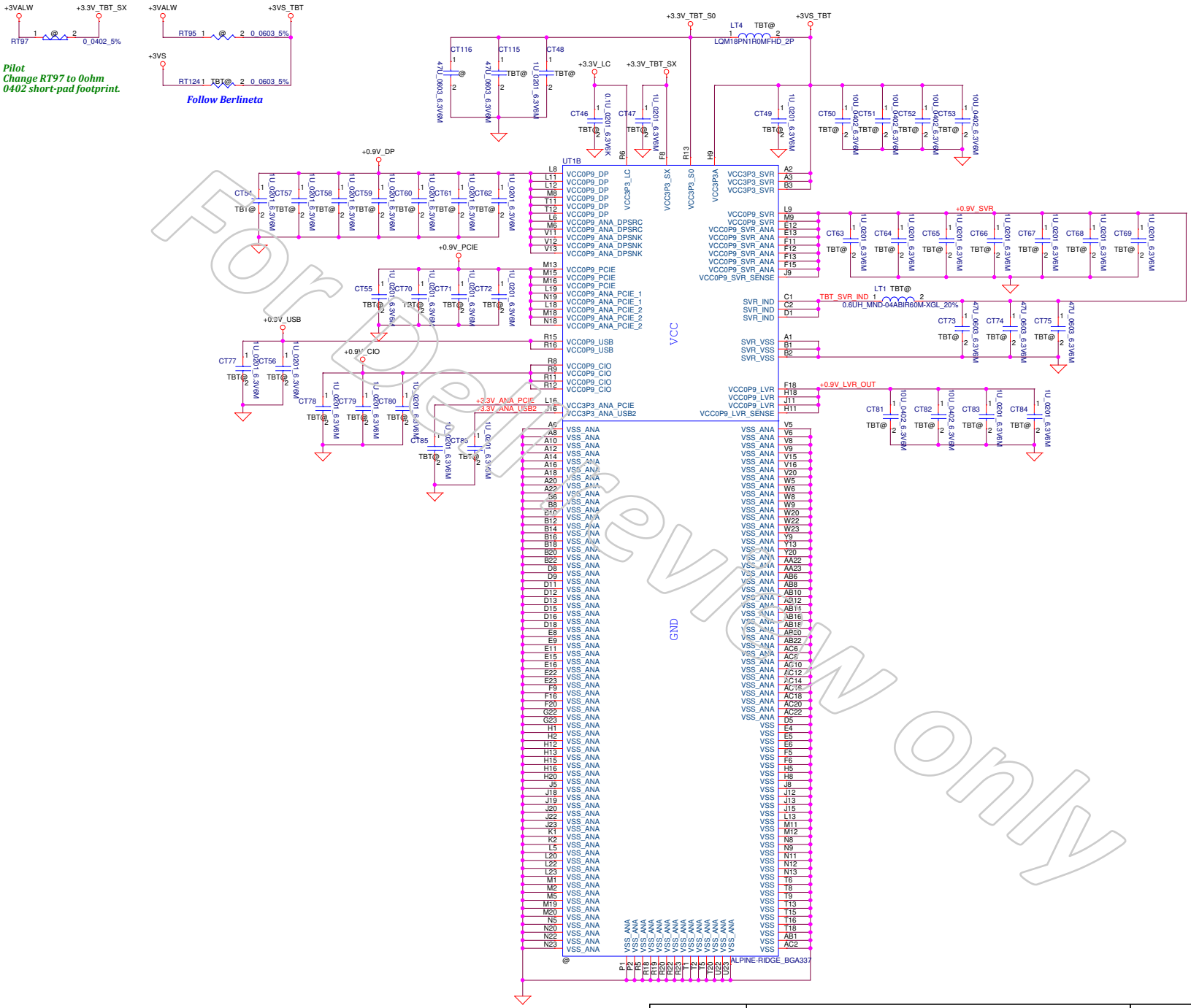
Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2016/09/18

Compal Electronics, Inc.

Title: Thunderbolt (1/2)

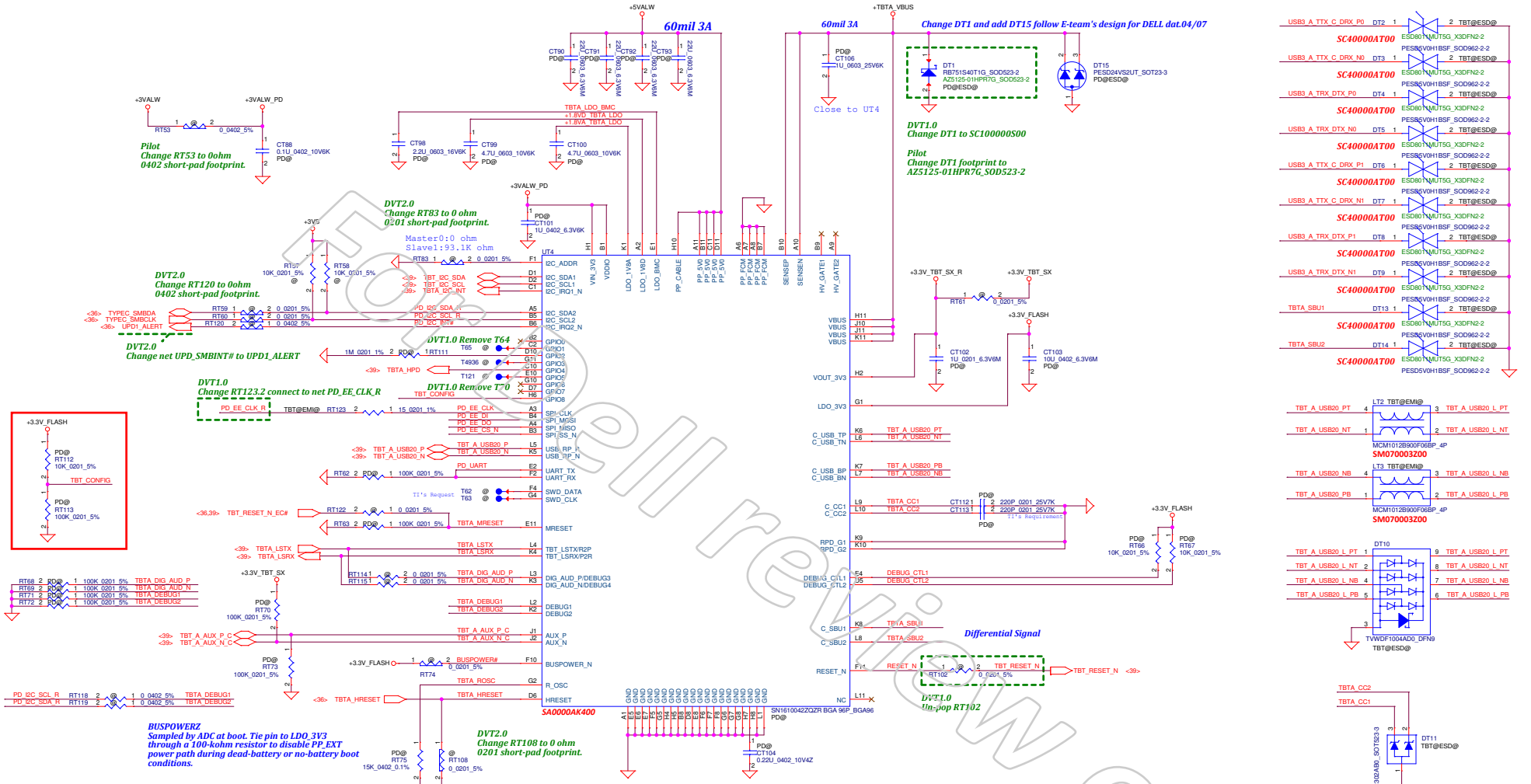
Size | Document Number: LA-E992P | Rev: 1.0(A00)

Date: Tuesday, July 25, 2017 | Sheet 39 of 77



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2016/09/18

Compal Electronics, Inc.	
Title	Thunderbolt (2/2)
Size	Document Number: LA-E992P
Rev	1.0(A00)
Date: Tuesday, July 25, 2017	Sheet 40 of 77



c. GPIO 8 (CONFIG) is a dedicated GPIO that must have a pull-up and pull-down resistor option included in the HW design.
When 82D has a SPI Flash Connected, the safest option is to use the "Infinite Retry" setting, which will prevent from loading an incorrect configuration. For this setting, GPIO 8 needs to be pulled to LDO_3V3, which effectively removes the divider (DIV = 1).

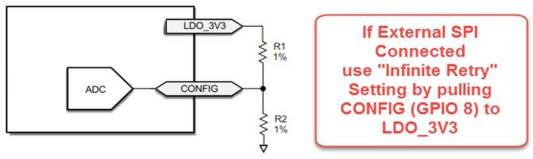


Figure 78. Factory Configuration Resistor Divider

Table 13. Factory Device Configuration Selection

DIV = R2/(R1+R2) (1)		Factory Device Configuration	Description
DIV_min	DIV_max		
0.70	1.00	7	Infinite boot retry from Flash to Host I/F cycles.

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/01/06	Deciphered Date 2016/09/18	Title: PD+USB3.1 type C
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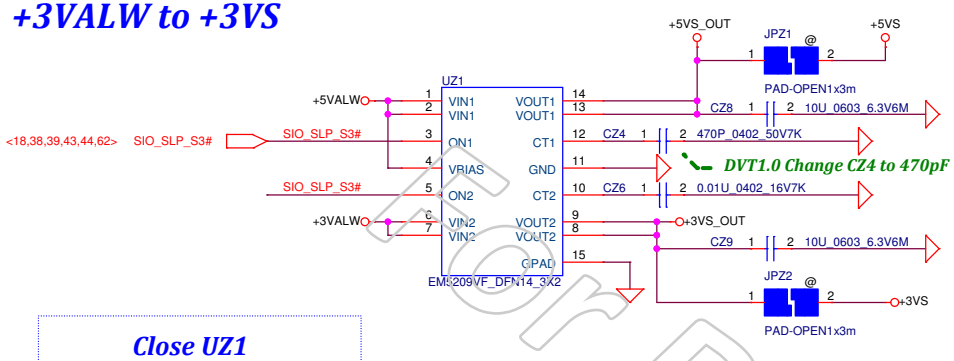
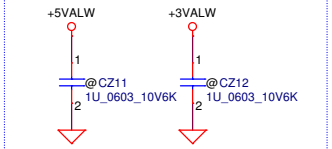
			Date: Tuesday, July 25, 2017 Sheet 41 of 77

+5VALW to +5VS
+3VALW to +3VS

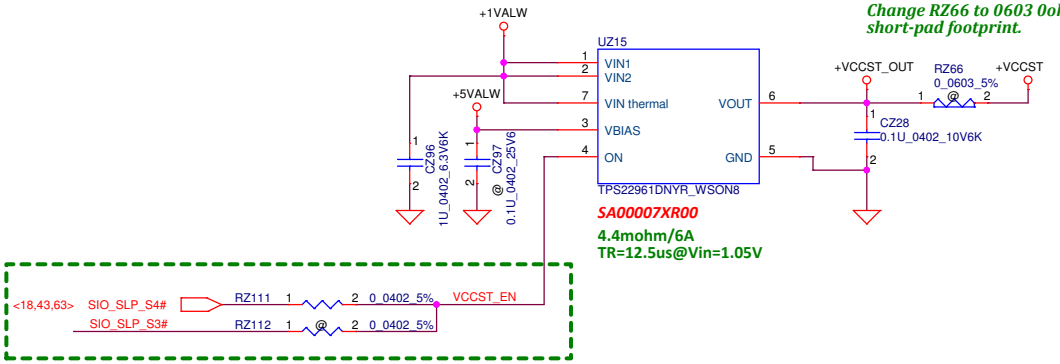


DVT1.0 Change CZ4 to 470pF

Close UZ1



+VCCST Load Switch

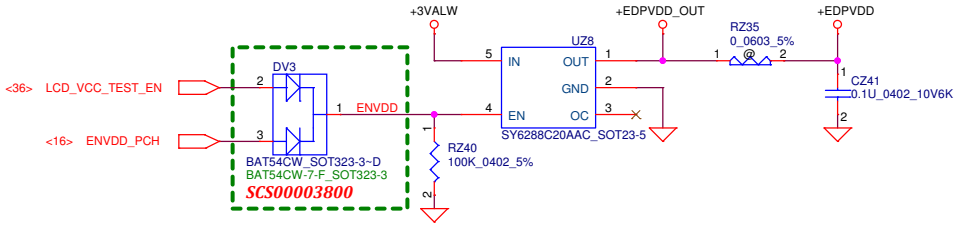


Pilot
Change RZ66 to 0603 0ohm short-pad footprint.

SA00007XR00
4.4mohm/6A
TR=12.5us@Vin=1.05V

DVT1.0
Add RZ111 connect to SIO_SLP_S4#
Add RZ112(@) connect to SIO_SLP_S3#
Add net VCCST_EN

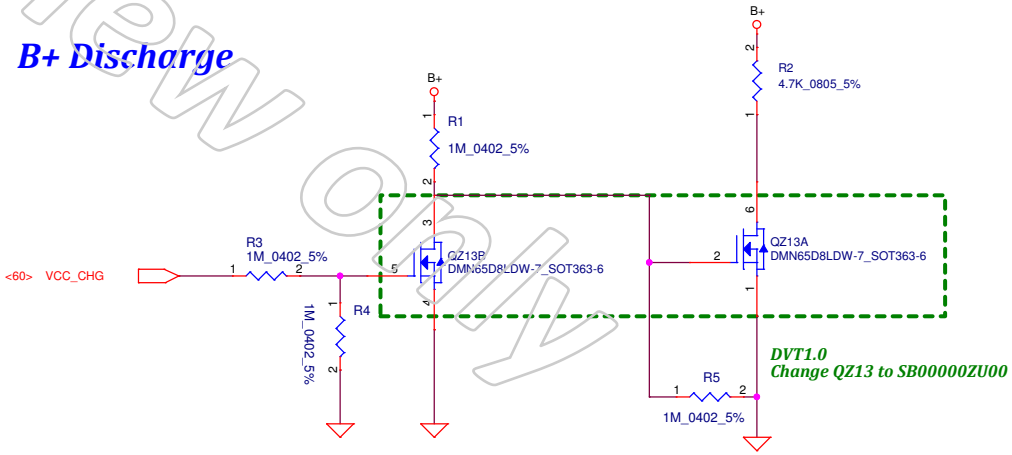
eDP Load Switch



Pilot
Change RZ35 to 0603 0ohm short-pad footprint.

DVT1.0
Change DV3 to SCS00003800.

B+ Discharge



DVT1.0
Change QZ13 to SB00000ZU00

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/08/25	Deciphered Date	2012/07/25
Title	SYS DC/DC Interface		
Size	Document Number		Rev
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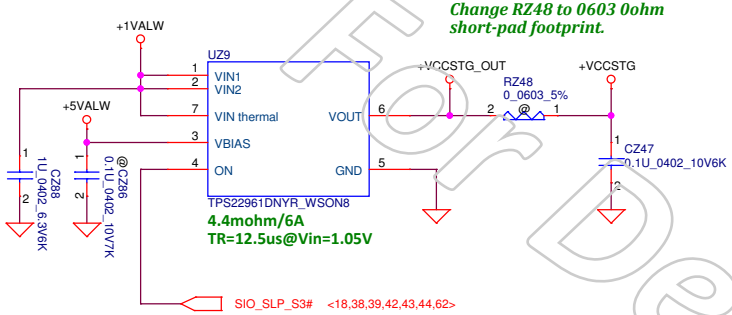
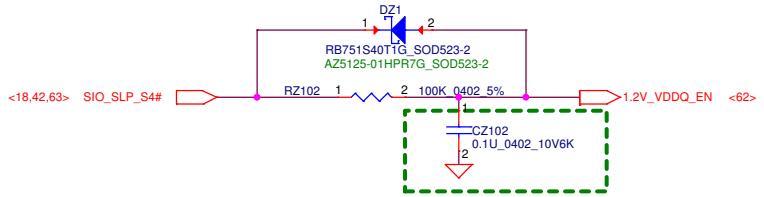
+VCCSTG Load Switch



Pilot
Change RZ48 to 0603 0ohm
short-pad footprint.

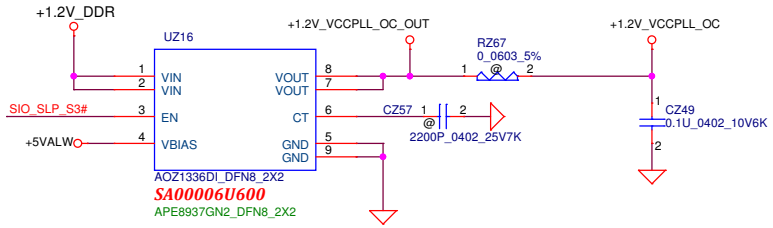
+1.2V_DDR Enable

Pilot
Change DZ1 footprint to AZ5125-01HPR7G_SOD523-2



DVT1.0 Change CZ102 to 0.1uF

+VCCPLL_OC Load Switch

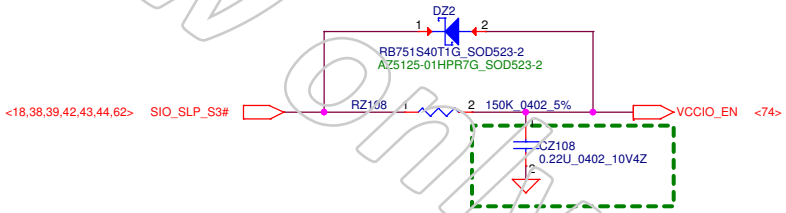


Pilot
Change RZ67 to 0603 0ohm
short-pad footprint.

Pilot
Change UZ16 form
APE8937GN2(SA000070L00) to
AOZ1336DI(SA00006U600), keep using
APE8937GN2_DFN8_2X2 footprint.

+VCCIO Enable

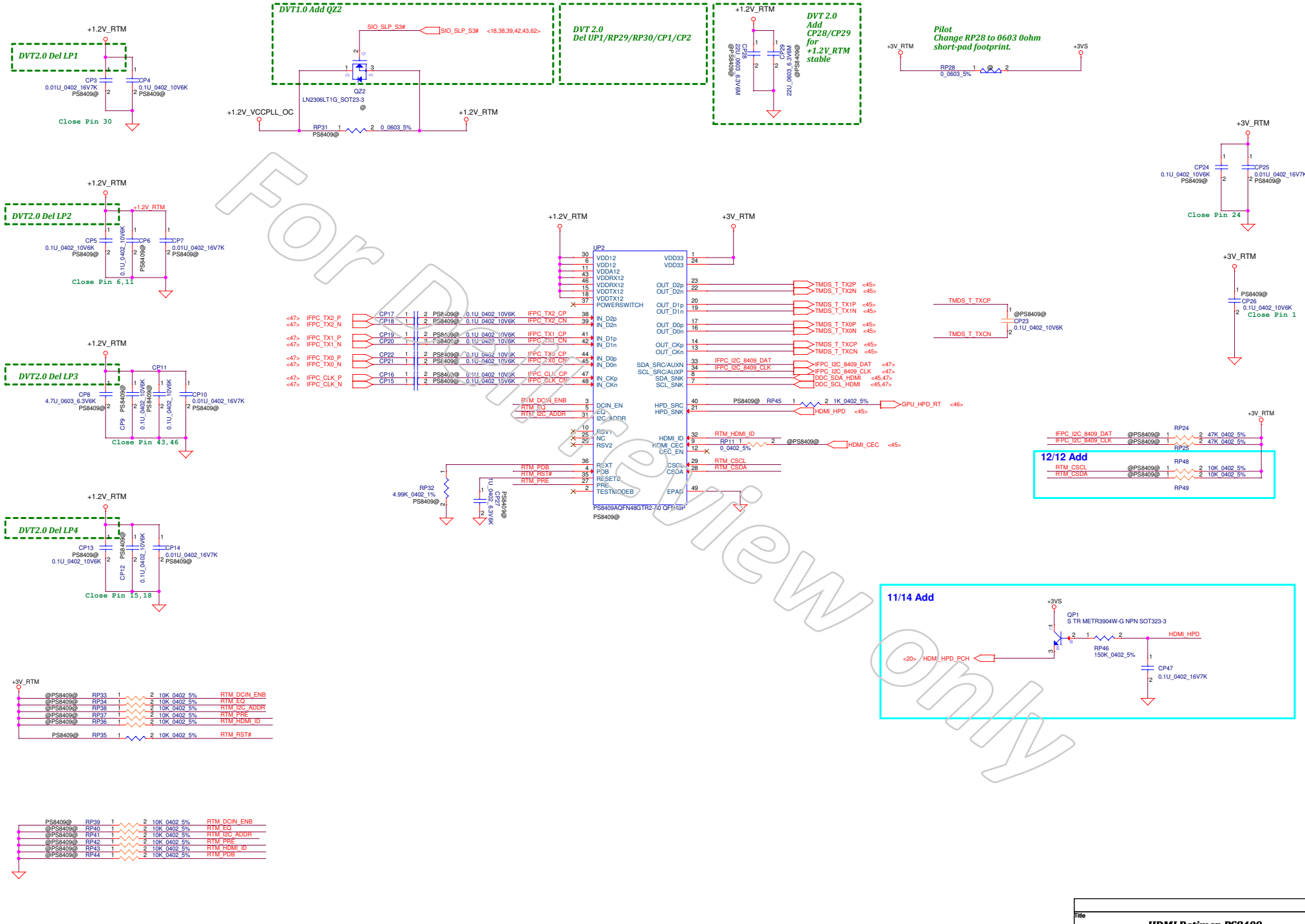
Pilot
Change DZ2 footprint to AZ5125-01HPR7G_SOD523-2



DVT1.0 Change CZ108 to 0.22uF

Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.	
Title	DC/DC/S0iX/CS
Size	Document Number: LA-E992P
Rev	1.0(A00)
Date: Tuesday, July 25, 2017	Sheet 43 of 77



Title	HDMI Retimer-PS8409
Size	C
Document Number	LA-E992P
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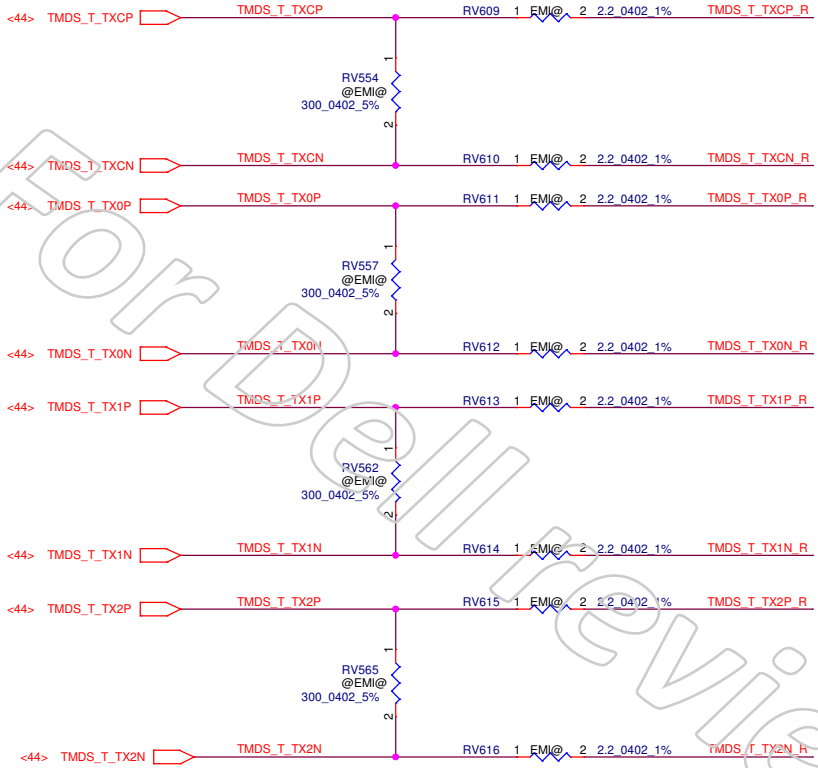
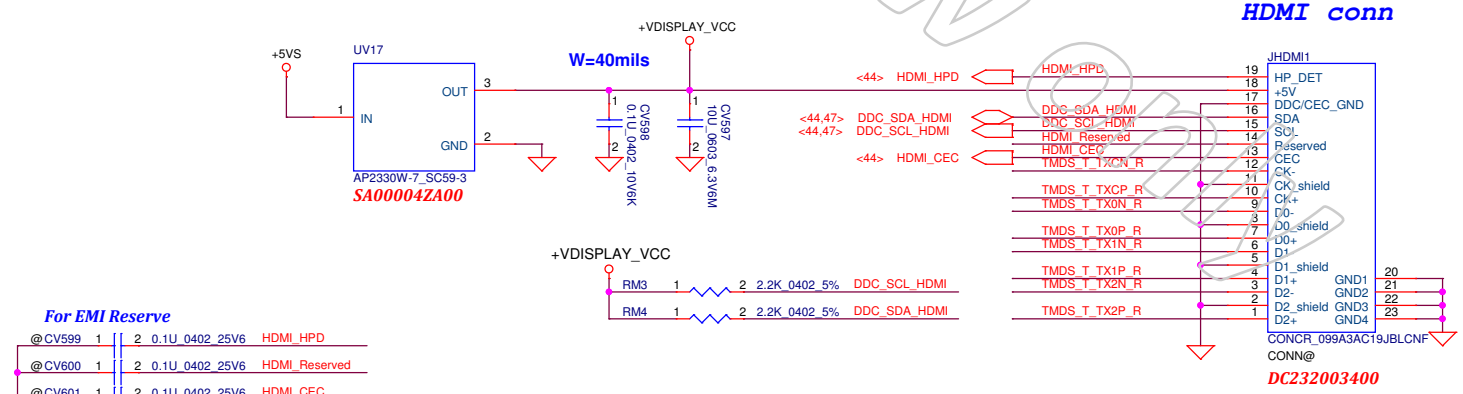
Place close to JHDMI1



HDMI conn



For EMI Reserve

Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: **HDMI**

Size | Document Number: **LA-E992P** | Rev: 1.0(A00)

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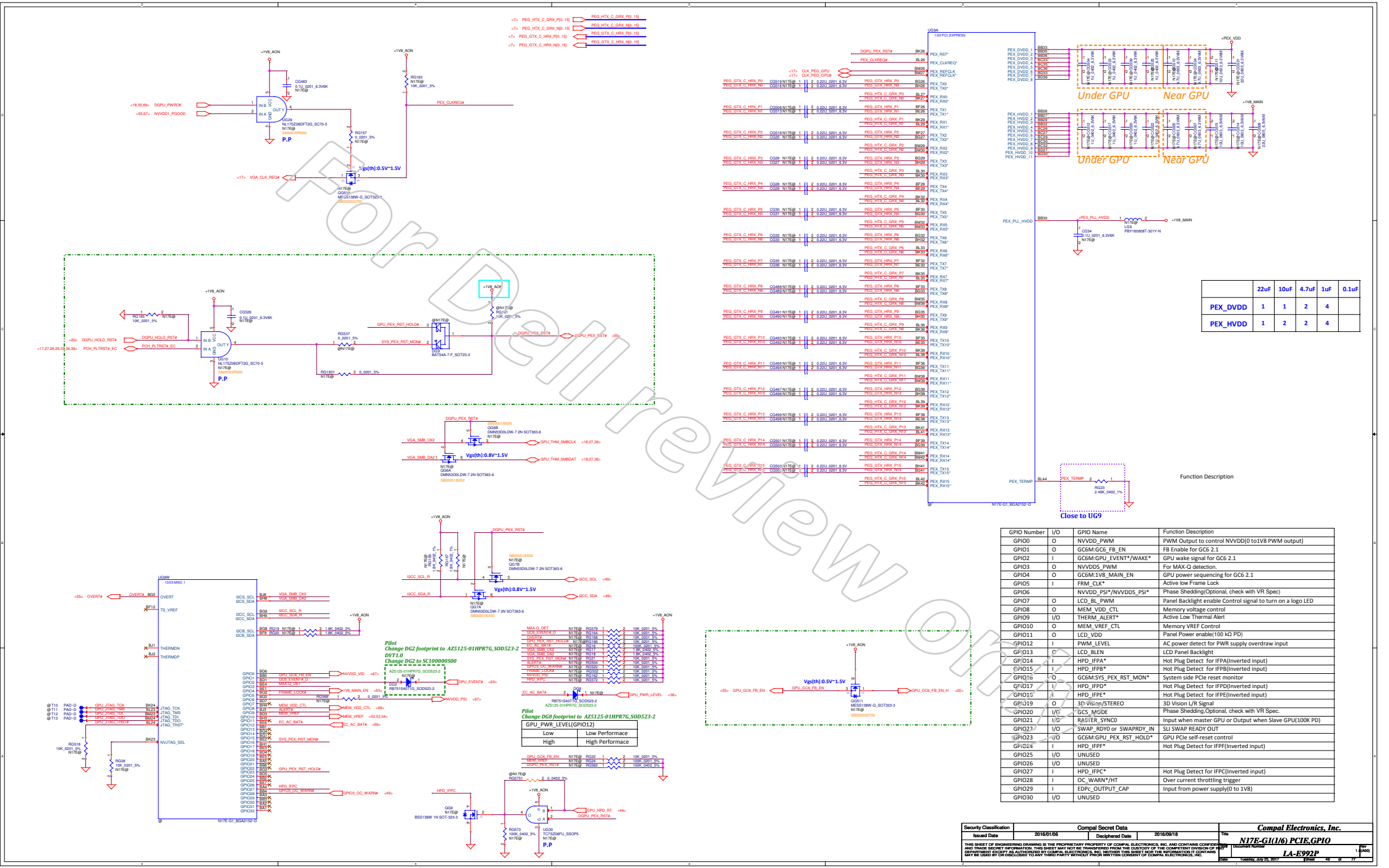
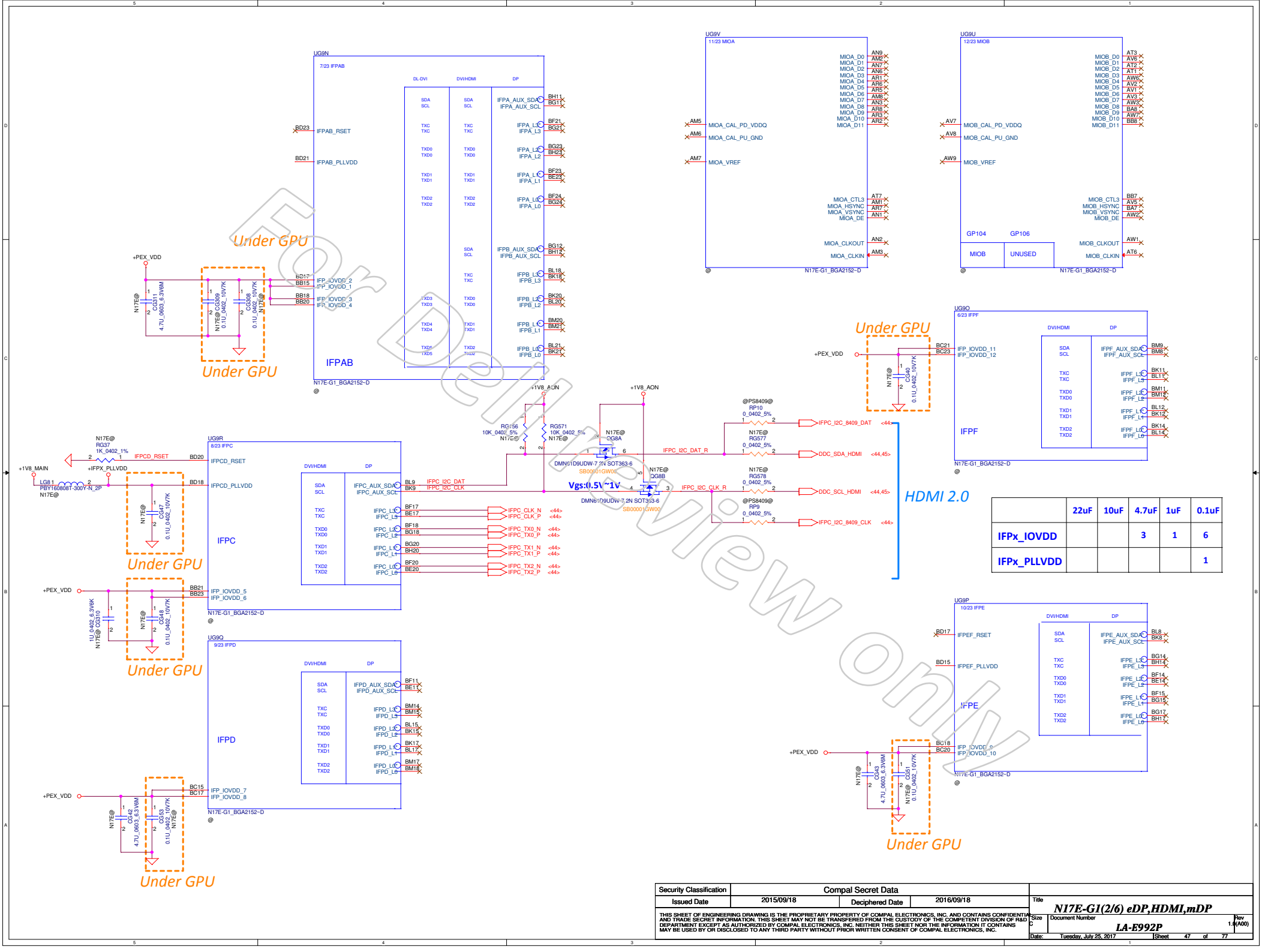


	22uF	10uF	4.7uF	1uF	0.1uF
PEX_DVDD	1	1	2	4	
PEX_HVDD	1	2	2	4	

GPIO Number	I/O	GPIO Name	Function Description
GPIO0	O	NVVDD_PWM	PWM Output to control NVVDD(0 to1V8 PWM output)
GPIO1	O	GC6M:GC6_FB_EN	FB Enable for GC6 2.1
GPIO2	I	GC6M:GPU_EVENT*/WAKE*	GPU wake signal for GC6 2.1
GPIO3	O	NVVDDS_PWM	For MAX-Q detection.
GPIO4	O	GC6M:1V8_MAIN_EN	GPU power sequencing for GC6 2.1
GPIO5	I	FRM_CLK*	Active low Frame Lock
GPIO6		NVVDD_PSI*/NVVDDS_PSI*	Phase Shedding(Optional, check with VR Spec)
GPIO7	O	LCD_BL_PWM	Panel Backlight enable Control signal to turn on a logo LED
GPIO8	O	MEM_VDD_CTL	Memory voltage control
GPIO9	I/O	THERM_ALERT*	Active Low Thermal Alert
GPIO10	O	MEM_VREF_CTL	Memory VREF Control
GPIO11	O	LCD_VDD	Panel Power enable(100 kΩ PD)
GPIO12	I	PWM_LEVEL	AC power detect for PWR supply overdraw input
GPIO13	O	LCD_BLEN	LCD Panel Backlight
GPIO14	I	HPD_IFPA*	Hot Plug Detect for IFPA(Inverted input)
GPIO15	I	HPD_IFPB*	Hot Plug Detect for IFPB(Inverted input)
GPIO16	O	GC6M:SYS_PEX_RST_MON*	System side PCIe reset monitor
GPIO17	I	HPD_IFPD*	Hot Plug Detect for IFPD(Inverted input)
GPIO18	I	HPD_IFPE*	Hot Plug Detect for IFPE(Inverted input)
GPIO19	O	3D_Vision/STEREO	3D Vision L/R Signal
GPIO20	I/O	GC5_MODE	Phase Shedding,Optional, check with VR Spec.
GPIO21	I/O	RASTER_SYNC0	Input when master GPU or Output when Slave GPU(100K PD)
GPIO22	I/O	SWAP_RDY0 or SWAPRDY_IN	SLI SWAP READY OUT
GPIO23	I/O	GC6M:GPU_PEX_RST_HOLD*	GPU PCIe self-reset control
GPIO24	I	HPD_IFPF*	Hot Plug Detect for IFPF(Inverted input)
GPIO25	I/O	UNUSED	
GPIO26	I/O	UNUSED	
GPIO27	I	HPD_IFPC*	Hot Plug Detect for IFPC(Inverted input)
GPIO28	I	OC_WARN*/HT	Over current throttling trigger
GPIO29	I	EDPc_OUTPUT_CAP	Input from power supply(0 to 1V8)
GPIO30	I/O	UNUSED	

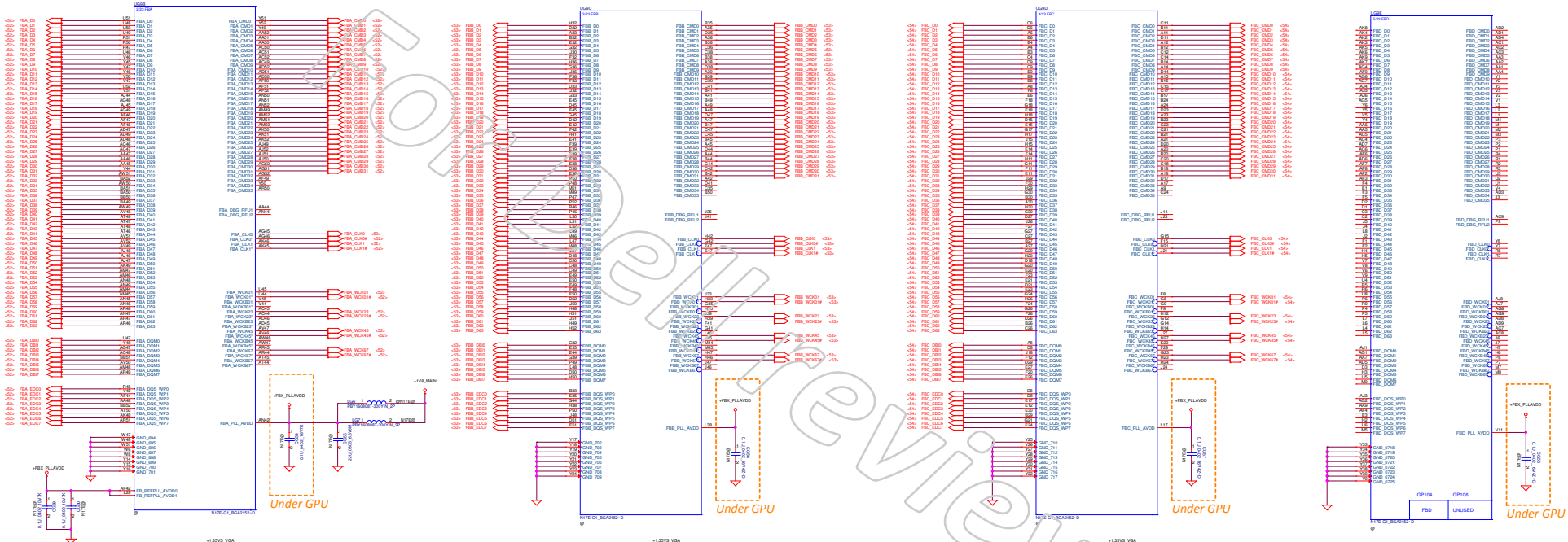
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/01/06	Deciphered Date 2016/09/18	Title: N17E-G1(1/6) PCIE,GPIO
			Document Number: LA-E992P
			Rev: 1.0(A00)
			Date: Tuesday, July 25, 2017 Sheet 46 of 77



	22uF	10uF	4.7uF	1uF	0.1uF
IFPx_IOVDD			3	1	6
IFPx_PLLVDD					1

Security Classification	Compal Secret Data		
Issued Date	2015/09/18	Deciphered Date	2016/09/18

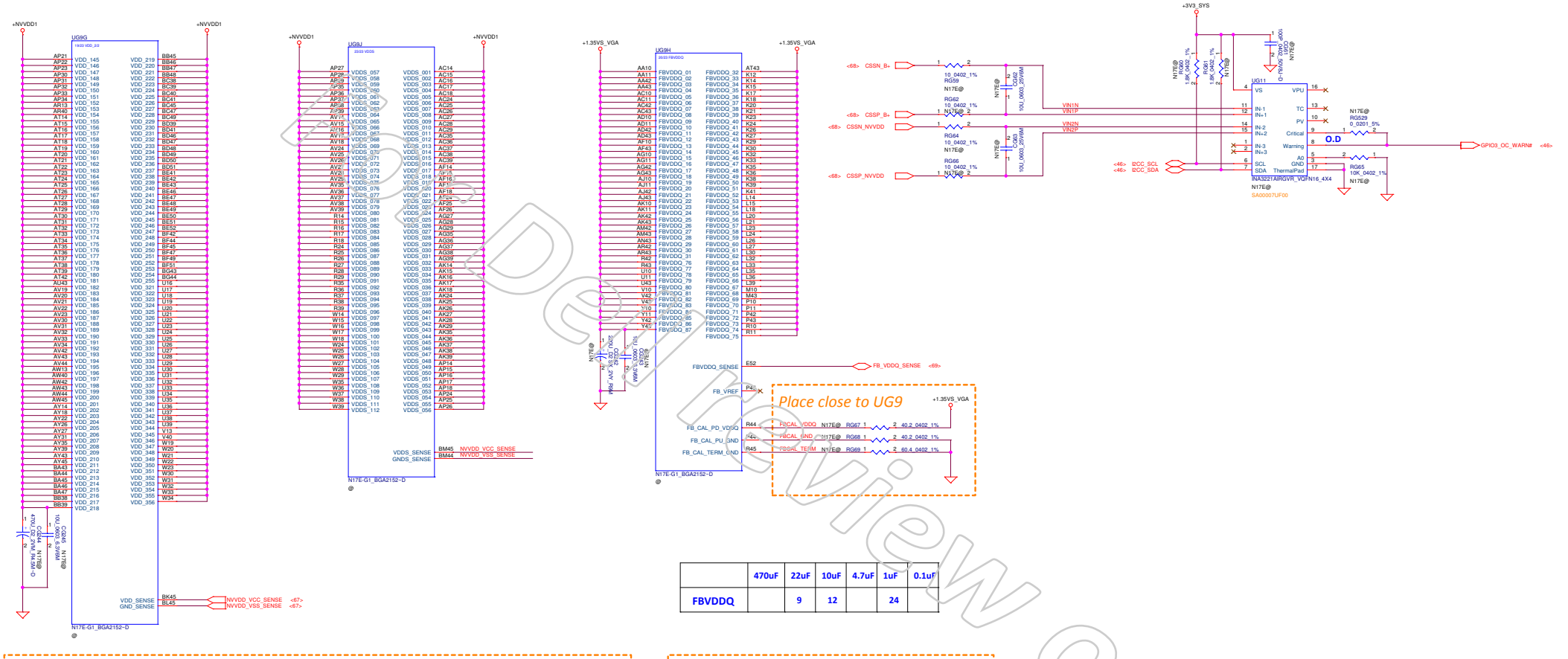
Title	N17E-G1(2/6) eDP,HDMI,mDP		
Size	Document Number		Rev
C	LA-E992P		1.0(A00)
Date:	Tuesday, July 25, 2017	Sheet	47 of 77



	22uF	10uF	4.7uF	1uF	0.1uF
FBx_PLL_AVDD					4

Security Classification	Compal Secret Data		
Issued Date	2015/09/18	Deciphered Date	2016/09/18

Title	N17E-GI(3/6) MEM interface		
Size	Document Number		Rev
Custom	LA-E992P		1.0(0A0)
Date:	Tuesday, July 26, 2016	Sheet	48 of 72



	470uF	22uF	10uF	4.7uF	1uF	0.1uF
FBVDDQ		9	12		24	

Security Classification	Compal Secret Data		
Issued Date	2015/09/18	Deciphered Date	2016/09/18

Title	N17E-G1(4/6) Power		
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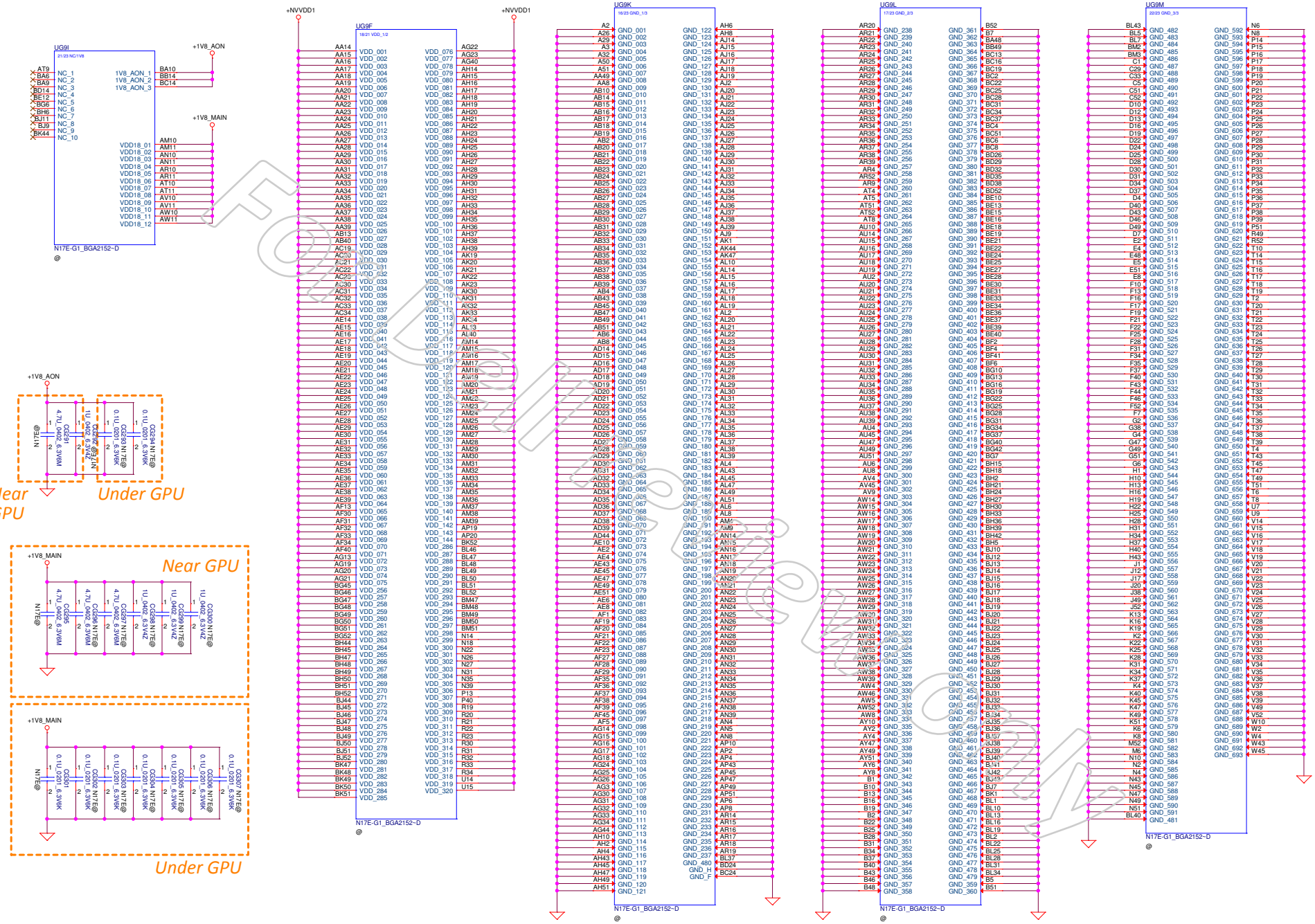

Security Classification	Compal Secret Data		
Issued Date	2015/09/18	Deciphered Date	2016/09/18

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Title: **N17E-G1(5/6) Power,GND**

Size	Document Number	Rev
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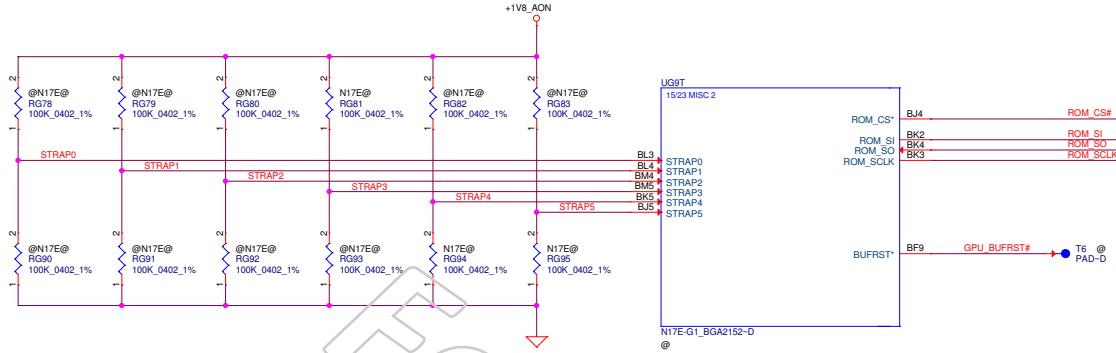
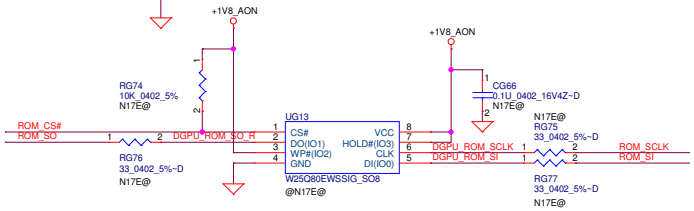




10/25 Need check high(SOIC or WSON)

Table 5.4 Display Link to SORx_EXPOSED Mapping for Down Designs

Total Display Links (HDMI, DP or DVI)	Total Enabled for Audio (HDMI, DP or DVI)	Is IFPD used? (Only supports eDP.)	See This Row of Table 5.5
3	2	YES	12
2	2	NO	12
2	1	YES	8
1	1	NO	8

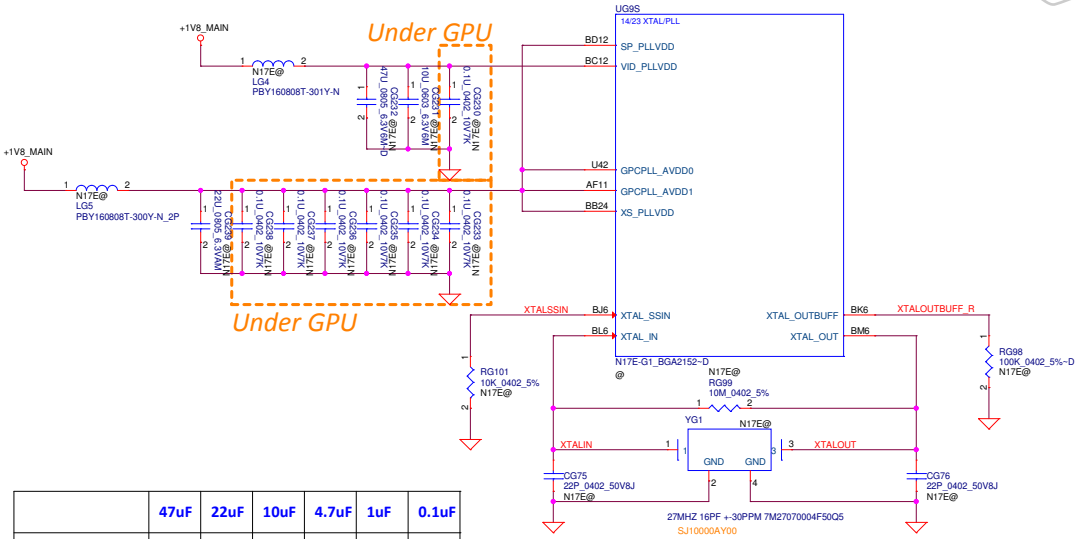
Row Index	Strap Pins see Note			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_ EXPOSED	SOR2_ EXPOSED	SOR1_ EXPOSED	SOR0_ EXPOSED
8	H	H	H	ENABLED	disabled	disabled	disabled

SMB_ALT_ADDR	
Low	Single GPU
High	Dual GPU

DEVID_SEL	
Low	Original Device ID
High	Re-brand Device ID

VGA_DEVICE	
Low	3D Device
High	VGA Device

PCIE_CFG	
Low	Normal signal swing
High	Reduce the signal amplitude



	47uF	22uF	10uF	4.7uF	1uF	0.1uF
VID_PLLVDD	1		1			1
SP_PLLVDD GPCPLL_AVDD		1				6

N17E-G1 VRAM	Strap0	Strap1	Strap2	Strap3	Strap4	Strap5	RAMCFG
SAMSUNG , K4G80325FB-HC25	L	L	L	H	L	L	0
MICRON , MT51J256M32HF-80:A	H	L	L	H	L	L	1
HYNIX , H5GQ8H24MJR-R4C	L	H	L	H	L	L	2

Table 2. N17E-G1 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35V and 1.55V[2]	Samsung	K4G80325FB-HC25	B-die	0x0	8 Gbps	N/A	Full	Production ready
		1.35V and 1.5V[2]	Micron	MT51J256M32HF-80:A	A-die	0x1	8 Gbps	N/A	Full	Production ready
		1.35V and 1.55V[2]	Hynix	H5GQ8H24MJR-R4C	M-die	0x2	8 Gbps	N/A	Full	Post production ready

Table 5.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Security Classification	Compal Secret Data		
Issued Date	2015/09/18	Deciphered Date	2016/09/18

Title	N17E-G1(6/6) strap pin,ROM		
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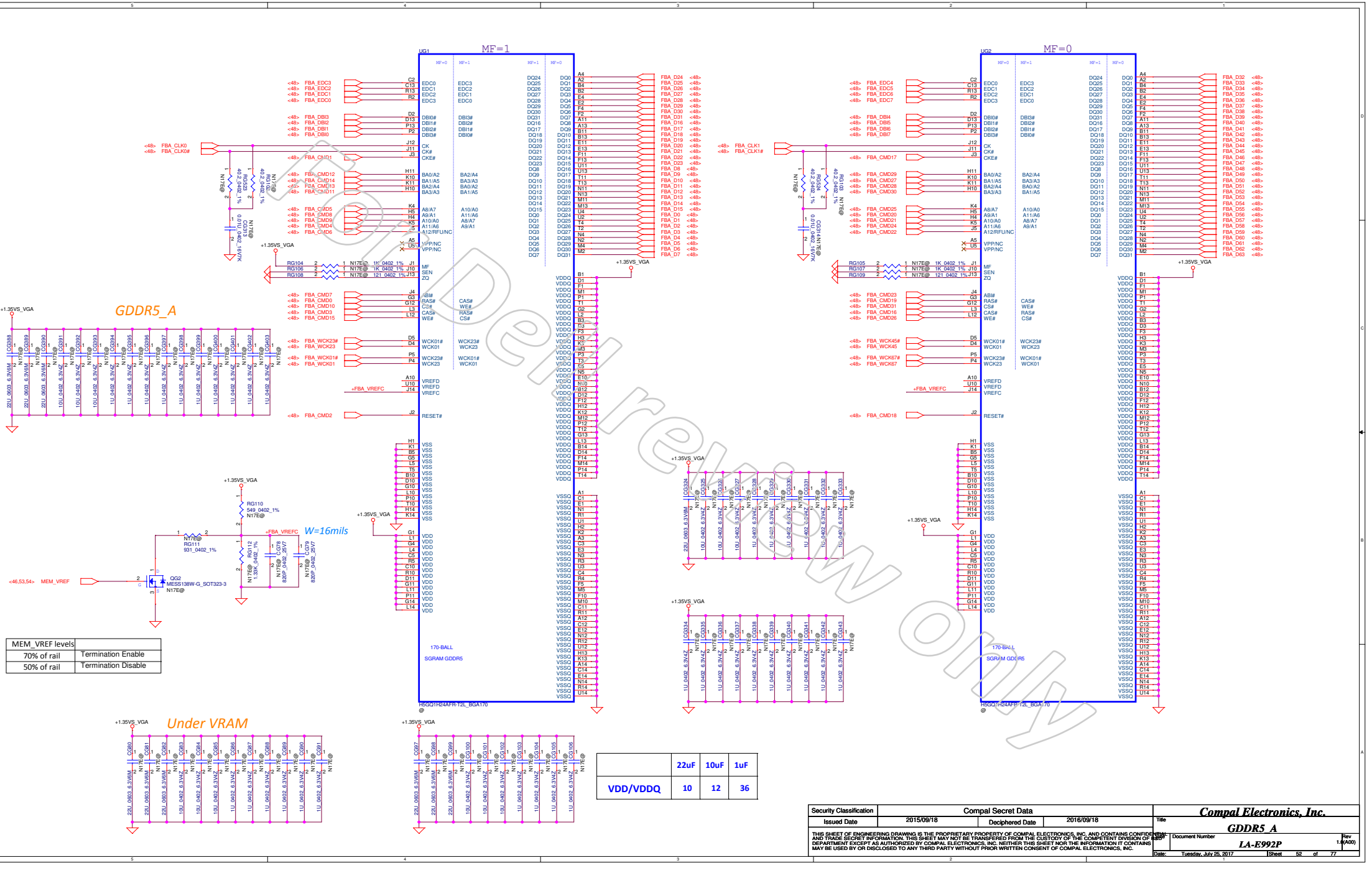
GDDR5_A
MF=1
MF=0
UG1
UG2
W=16mils
Under VRAM
170-BALL
SGRAM GDDR5
H5GQ1H24AFR-T2L_BGA170
MEM_VREF levels
70% of rail
Termination Enable
50% of rail
Termination Disable
VDD/VDDQ
22uF
10uF
1uF
10
12
36
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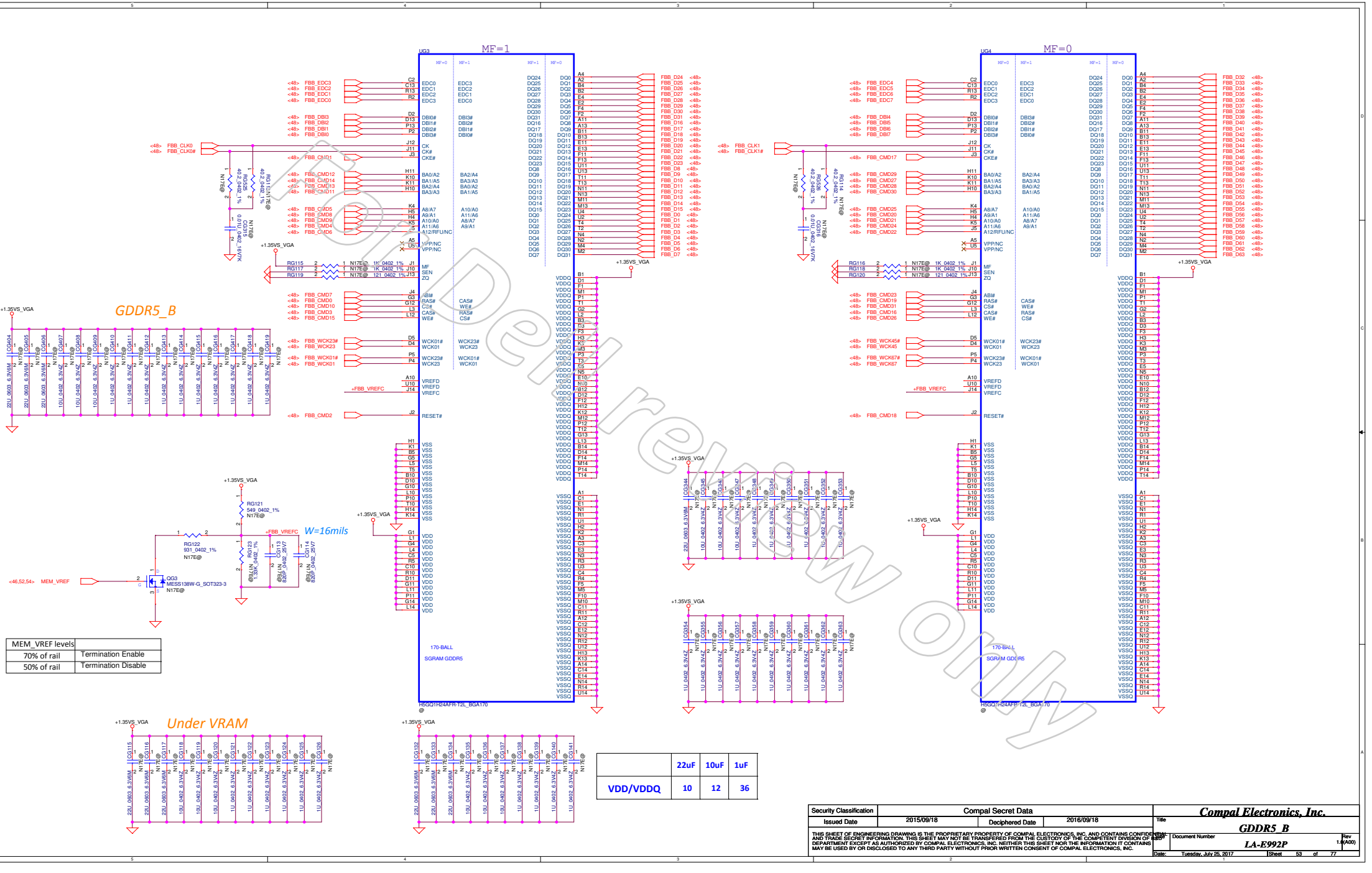

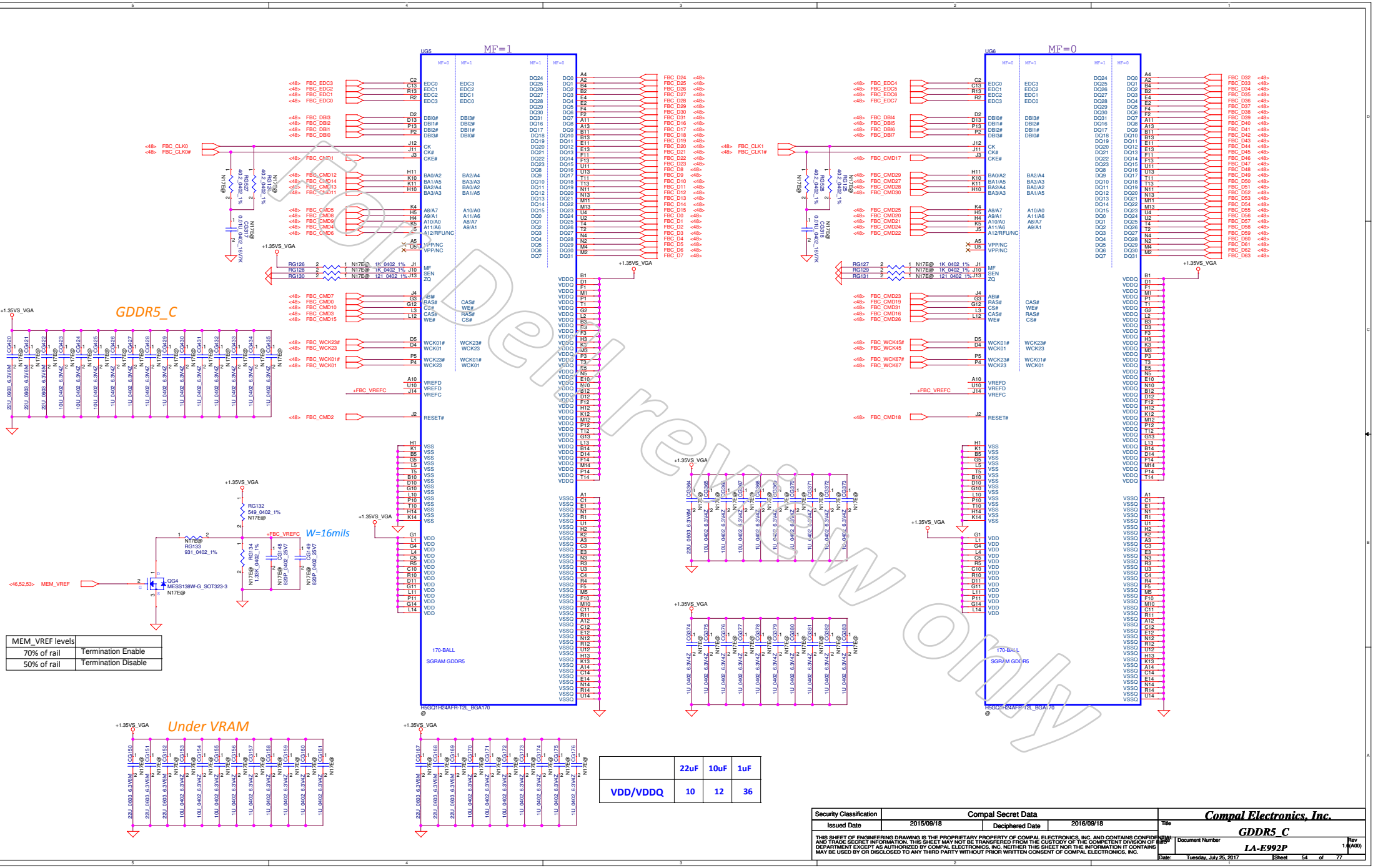

Security Classification	Compal Secret Data
Issued Date	2015/09/18
Deciphered Date	2016/09/18

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Title	GDDR5_C
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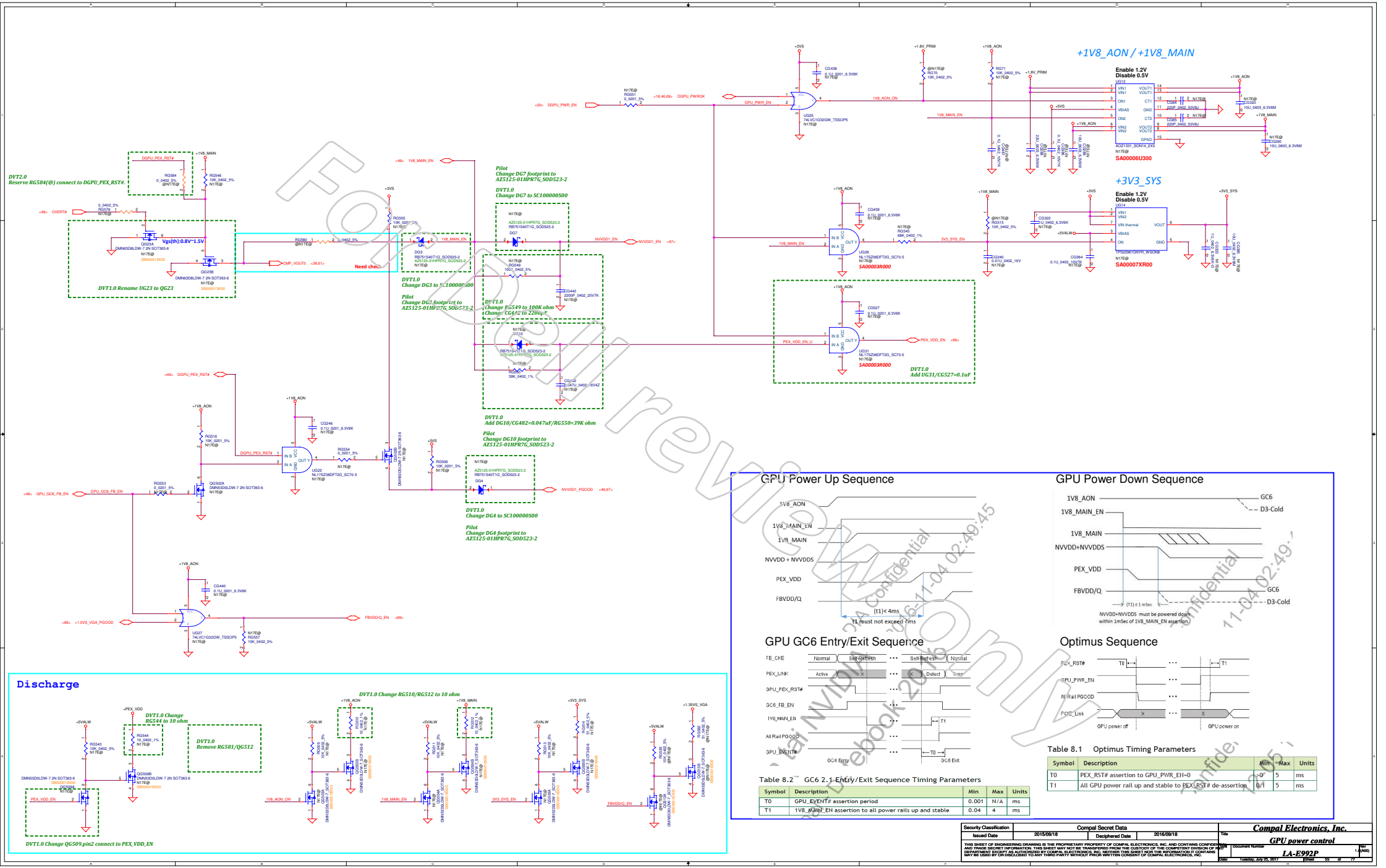

Table 8.2 GC6 2.1 Entry/Exit Sequence Timing Parameters

Symbol	Description	Min	Max	Units
T0	GPU_EVENT# assertion period	0.001	N/A	ms
T1	1V8_MAIN_EN assertion to all power rails up and stable	0.04	4	ms

Table 8.1 Optimus Timing Parameters

Symbol	Description	Min	Max	Units
T0	PEX_RST# assertion to GPU_PWR_EN=0	>0	5	ms
T1	All GPU power rail up and stable to PEX_RST# de-assertion	0.1	5	ms

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MODEL NAME : ***CKF50/CKA50***

PCB NO : ***LA-E992P***

Bom Structure

ZZZ PCB@

PCB CKA50 LA-E992P LS-E992P/E993P 02

DAZ21J00310

CPU

UH1 I7_QLM5@ — *R1* — KBL-H_QLM5 — *SA0000AD70L*

UH1 I5_QLM7@ — *R1* — KBL-H_QLM7 — *SA0000AD80L*

UH1 I7_MP@ — *R3* — KBL-H_SR32Q — *SA0000AD72L*

UH1 I5_MP@ — *R3* — KBL-H_SR32S — *SA0000AD82L*

PCH

UH2 QLF9@ — PCH_QLF9 — *SA0000ADB0L*

UH2 SR30W@ — PCH_SR30W — *SA0000ADB2L*

GPU

UG9 N17E_G1@ — N17E-G1-A1 — *SA00009PM1L*

Samsung 6G — X7673331L07 : S6G@

UG1	K4G80325FB-HC25 S6G@	*SA00009TA1L*	RG90 100K_0402_1% S6G@ *SD034100380*
UG2	K4G80325FB-HC25 S6G@	*SA00009TA1L*	RG91 100K_0402_1% S6G@ *SD034100380*
UG3	K4G80325FB-HC25 S6G@	*SA00009TA1L*	RG92 100K_0402_1% S6G@ *SD034100380*
UG4	K4G80325FB-HC25 S6G@	*SA00009TA1L*	
UG5	K4G80325FB-HC25 S6G@	*SA00009TA1L*	
UG6	K4G80325FB-HC25 S6G@	*SA00009TA1L*	

Micron 6G — X7673331L09 : M6G@

UG1	MT51J256M32HF-80:A M6G@	*SA00009TI1L*	RG78 100K_0402_1% M6G@ *SD034100380*
UG2	MT51J256M32HF-80:A M6G@	*SA00009TI1L*	RG91 100K_0402_1% M6G@ *SD034100380*
UG3	MT51J256M32HF-80:A M6G@	*SA00009TI1L*	RG92 100K_0402_1% M6G@ *SD034100380*
UG4	MT51J256M32HF-80:A M6G@	*SA00009TI1L*	
UG5	MT51J256M32HF-80:A M6G@	*SA00009TI1L*	
UG6	MT51J256M32HF-80:A M6G@	*SA00009TI1L*	

Hynix 6G — X7673331L08 : H6G@

UG1	H5GQ8H24MJR-R4C H6G@	*SA00009TM1L*	RG90 100K_0402_1% H6G@ *SD034100380*
UG2	H5GQ8H24MJR-R4C H6G@	*SA00009TM1L*	RG79 100K_0402_1% H6G@ *SD034100380*
UG3	H5GQ8H24MJR-R4C H6G@	*SA00009TM1L*	RG92 100K_0402_1% H6G@ *SD034100380*
UG4	H5GQ8H24MJR-R4C H6G@	*SA00009TM1L*	
UG5	H5GQ8H24MJR-R4C H6G@	*SA00009TM1L*	
UG6	H5GQ8H24MJR-R4C H6G@	*SA00009TM1L*	

X43		431A7631L51 SMT MB AE992 CKF50 KBL I5 N17EG1 6G	431A7631L52 SMT MB AE992 CKF50 KBL I7 N17EG1 6G	431A7631L01 SMT MB AE992 CKA50 KBL I7 N17EG1 PTT 6G	431A7631L02 SMT MB AE992 CKA50 KBL I5 N17EG1 PTT 6G
PCB P/N	PCB@	V	V	V	V
Project ID	AMN@			V	V
	FSTR@	V	V		
CPU P/N	I5_MP@	V			V
	I7_MP@		V	V	
	I5_QLM7@				
	I7_QLM5@				
PCH P/N	SR30W@	V	V	V	V
	QLF9@				
GPU ID Model ID	UMA@				
	N17P_G0@				
	N17P_G1@				
	N17E_G1@	V	V	V	V
N17E GPU	N17E@	V	V	V	V
Phase ID Board ID	EVT@				
	DVT1@				
	DVT2@				
	PILOT@	V	V	V	V
TBT	TBT@	V	V	V	V
TPS65982D	PD@	V	V	V	V
PS8409	PS8409@	V	V	V	V
DP to VGA	VGA@			V	V
Free Fall sensor	FFS@			V	V
TPM	TPM@				
	NON_TPM@	V	V	V	V
E991/E992 TPM Option	991@TPM@				
	992@TPM@				
USB3.0 re-driver	PARADE@	V	V	V	V
	PERICOM@				
Touch Screen	TS@	V	V	V	V
XDP	XDP@	V	V	V	V
Debug LED&Button	DEBUG@				
USB Port 100u Cap	RBOM@				
Connector	CONN@				
Reserve	@N17E@				
	@PS8409@				

X4E		X4EA7631L51 SMT EMC FOR EE N17E AE992 CKF50	X4EA7631L01 SMT EMC FOR EE N17E AE992 CKA50
Touch FP with power buttoN	FP1@EMI@	V	V
	FP1@ESD@	V	V
Gernal EMI	EMI@	V	V
Gernal ESD	ESD@	V	V
TBT	TBT@EMI@	V	V
	TBT@ESD@	V	V
PD-TPS65982D	PD@ESD@	V	V
Touch Screen	TS@EMI@	V	V
	TS@ESD@	V	V
RF	RF@	V	V
VGA EMI	VGA@EMI@		V
991 PCH SPI CLK	991@EMI@		
992 PCH SPI CLK	992@EMI@	V	V
Reserve	@EMI@		
	@ESD@		
	@RF@		
	@TS@EMI@		

X76	X7673331L07 ALT. GROUP PARTS SAMSUNG 6G VRAM CKA50	X7673331L08 ALT. GROUP PARTS HYNIX 6G VRAM CKA50	X7673331L09 ALT. GROUP PARTS MICRON 6G VRAM CKA50
S6G@	√		
H6G@		√	
M6G@			√

Security Classification	Compal Secret Data		
Issued Date	2013/04/10	Deciphered Date	2014/05/01

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Title: **NOTE**

Size | Document Number: **LA-E992P** | Rev: 1.0(A00)

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Title: ***NOTE***		
Size	Document Number: ***LA-E992P***	Rev: 1.0(A00)
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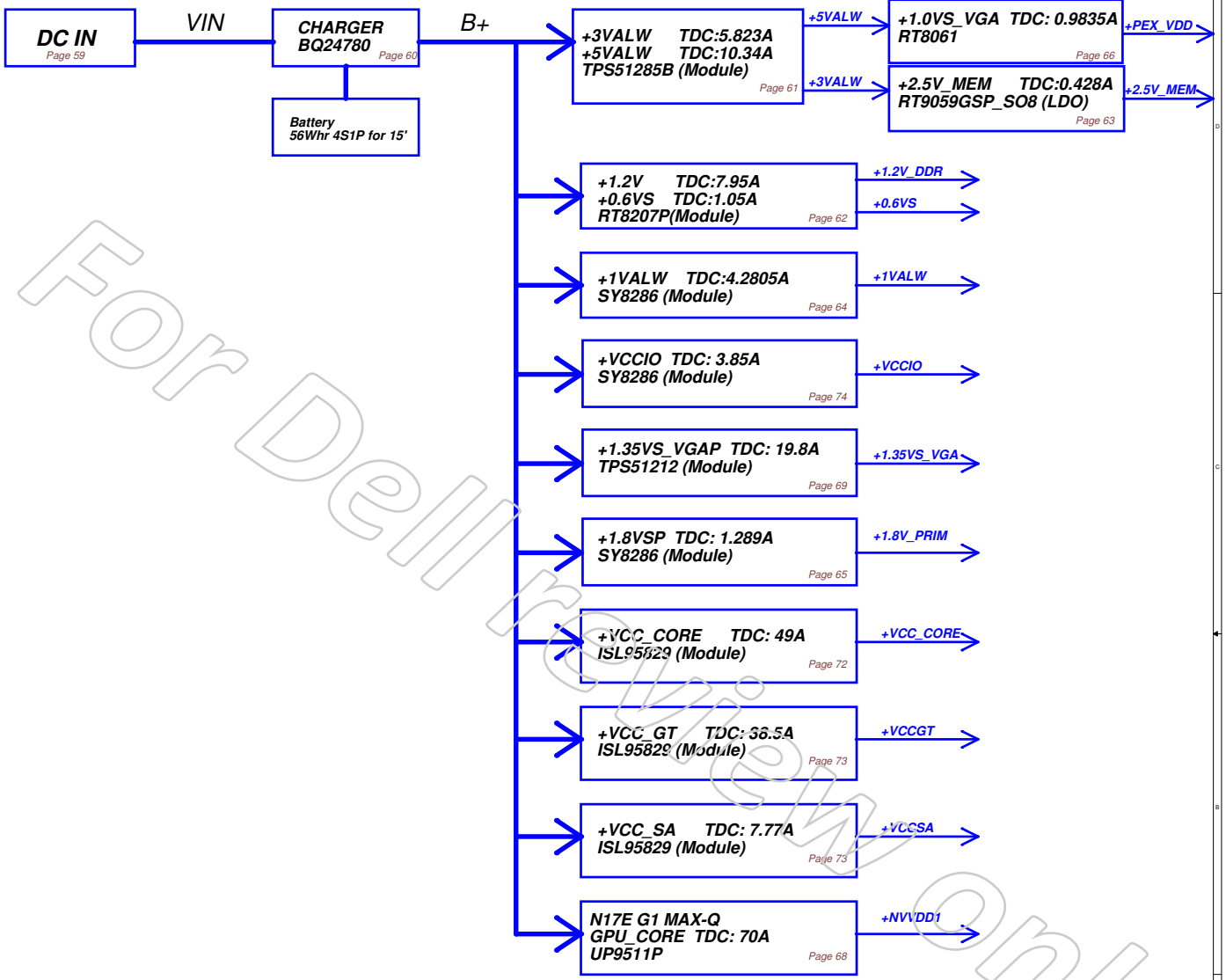

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/08/25	Deciphered Date	2012/07/25
Title	Power Block Diagram		
Document Number	LA-E992P		Rev 0.3(002)
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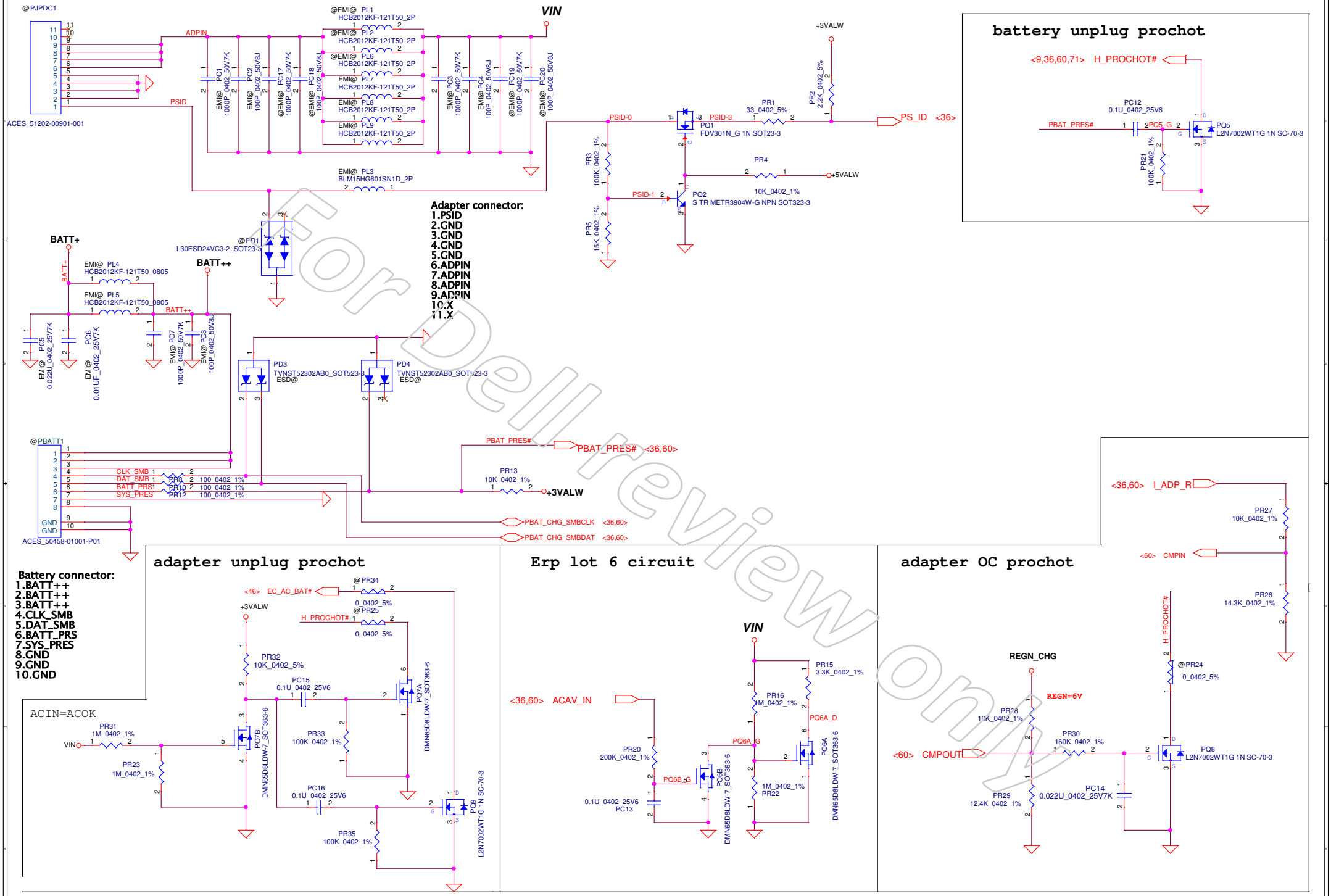

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Issued Date	2015/09/18	Deciphered Date	2016/09/18

Compal Electronics, Inc.	
Title	PWR-DCIN / BATT CONN / OTP
Size	Document Number: LA-E992P
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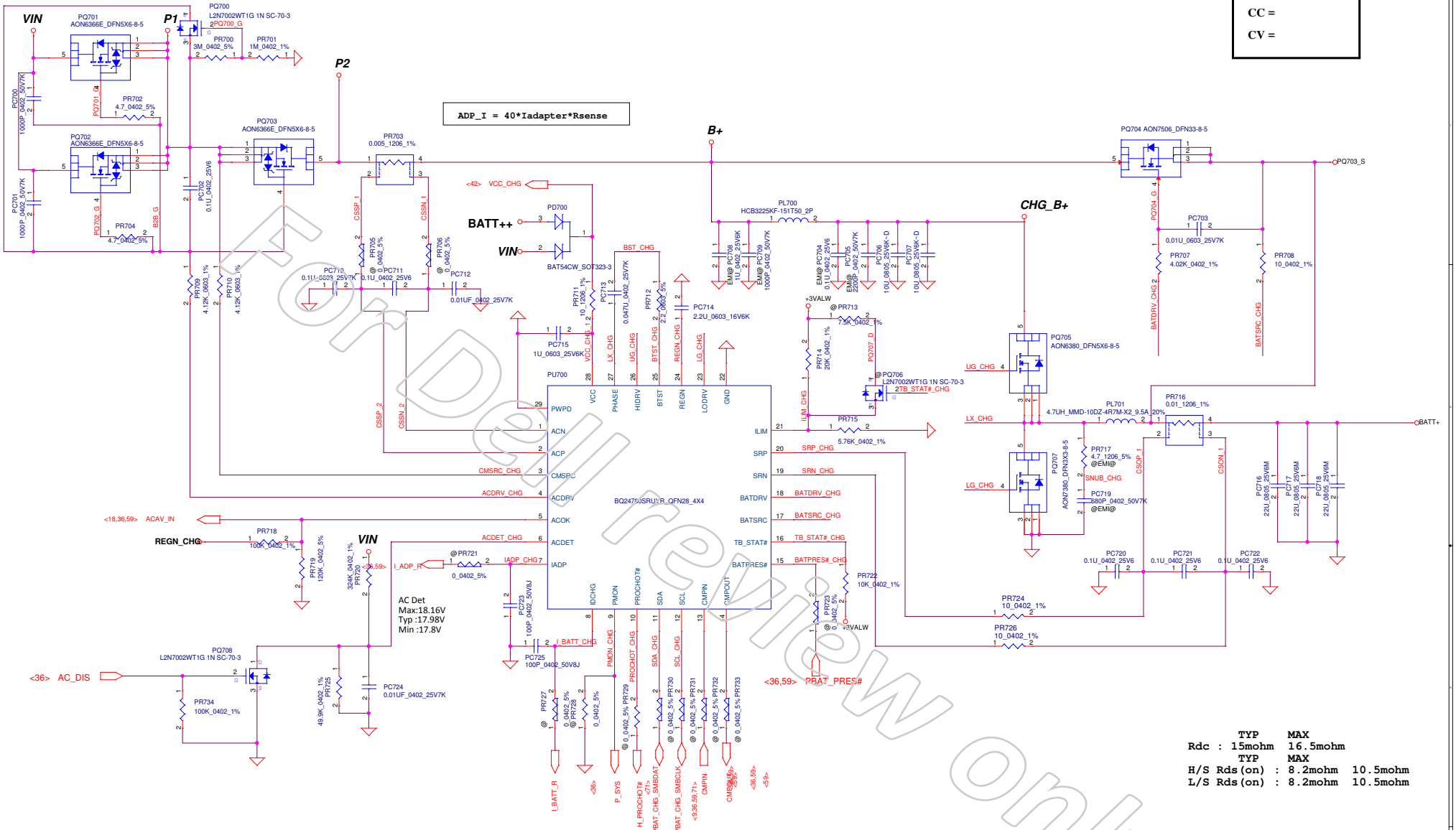

Security Classification	Compal Secret Data		
Issued Date	2015/09/18	Deciphered Date	2016/09/18

Compal Electronics, Inc.	
Title	PWR_CHARGER
Size	Document Number: LA-E992P
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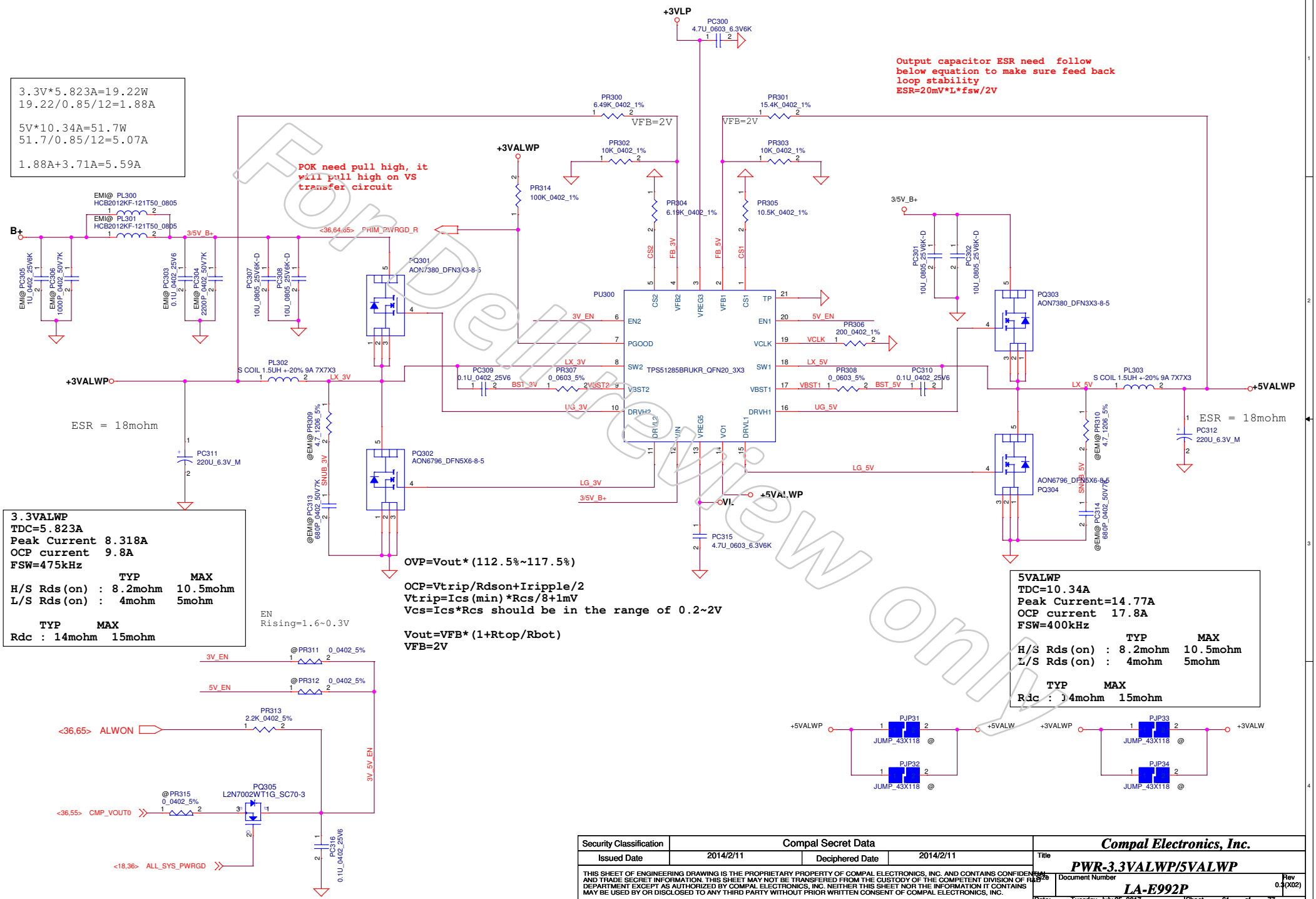

Security Classification	Compal Secret Data		
Issued Date	2014/2/11	Deciphered Date	2014/2/11

Compal Electronics, Inc.	
Title	PWR-3.3VALWP/5VALWP
Size	B
Document Number	LA-E992P
Rev	0.3(X02)
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Input Current: 0.935A
1.2V*7.95A/0.85/12V=0.935

Pin19 need pull separate from +1.2VP.
If you have +1.2V and +0.6V sequence question,
you can change from +1.2VP to +1.2VS.

0.6VSP
TDC 1.05A
Peak Current 1.5A

PR201=20.5K for OCP=15A,
Ron=15.8mohm, delta_I=3.94A

1.2VP
TDC=7.95A
Ipeak=11.356A
OCP=15A
Switching Frequency: 550kHz

	TYP	MAX
DCR :	6.7mohm	7.4mohm

OVP: 110%~120%
VFB=0.75V, Vout=1.2V

	TYP	MAX
H/S Rds(on) :	22.7mohm	32mohm
L/S Rds(on) :	13mohm	15.8mohm

Mode	Level	+0.6VSP	VTTREF_1.2V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

RILMT=ILIMIT*Ron/10uA
where RILMT=PR201=20.5K,Ron=15.8m
=>ILIMIT=15A

Security Classification	Compal Secret Data		
Issued Date	2015/09/18	Deciphered Date	2016/09/18

Compal Electronics, Inc.

Title: PWR-1.2VP/0.6VSP

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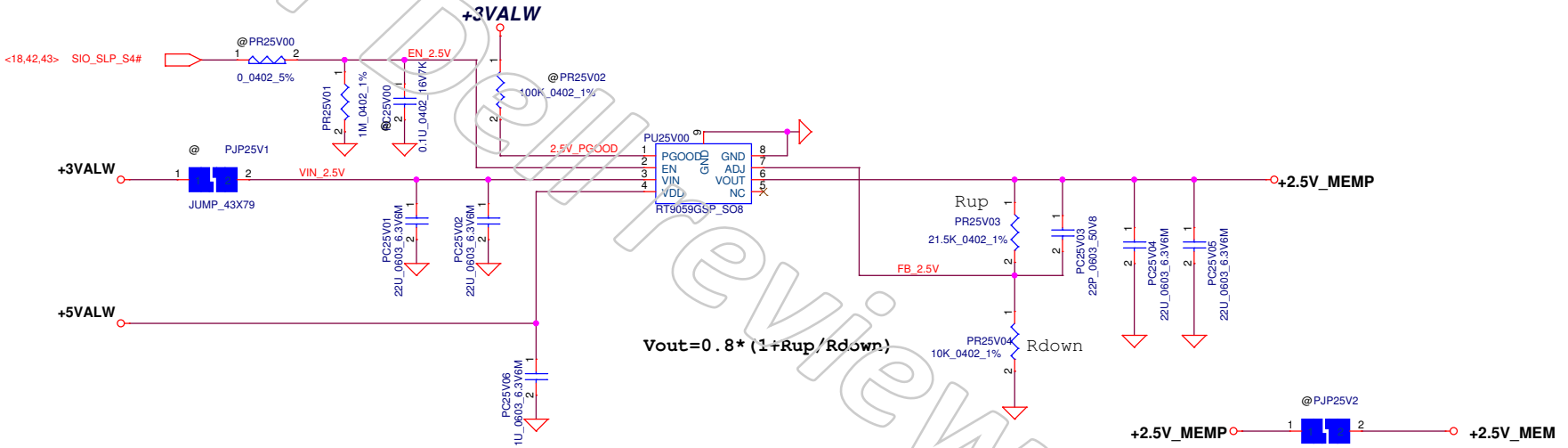
Input Current:0.42A

2.5*0.428=1.07W
1.07/0.85/3=0.42A



+2.5V_MEM
TDC 0.428A
Peak Current 0.612A
OCP Current 3.5A

Security Classification	Compal Secret Data		
Issued Date	2015/09/18	Deciphered Date	2016/09/18

Compal Electronics, Inc.

Title: PWR_+2.5V_MEM

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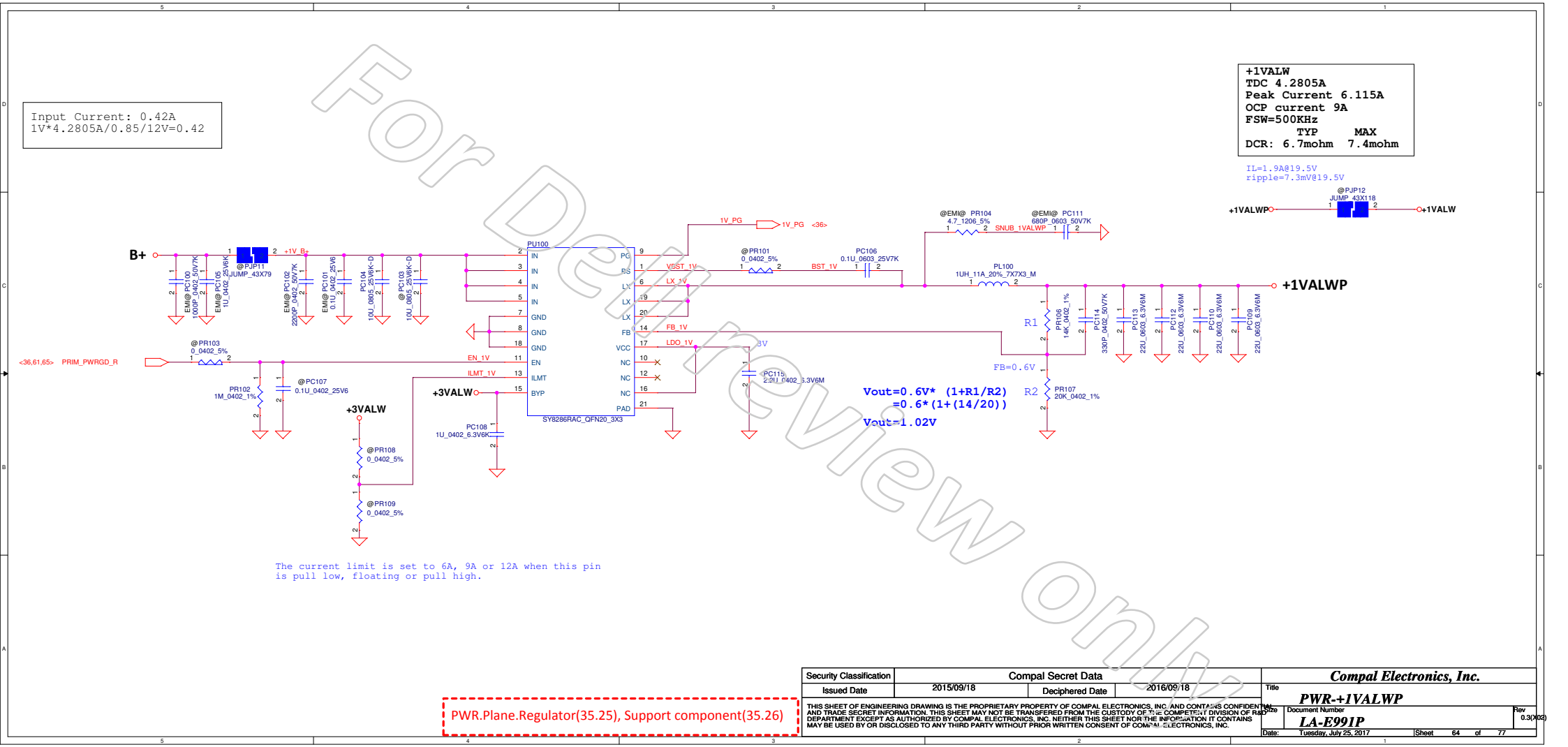

Security Classification	Compal Secret Data		
Issued Date	2015/09/18	Deciphered Date	2016/09/18

Compal Electronics, Inc.			
Title: PWR-+1VALWP			
Size	Document Number: LA-E991P		Rev: 0.3(X02)
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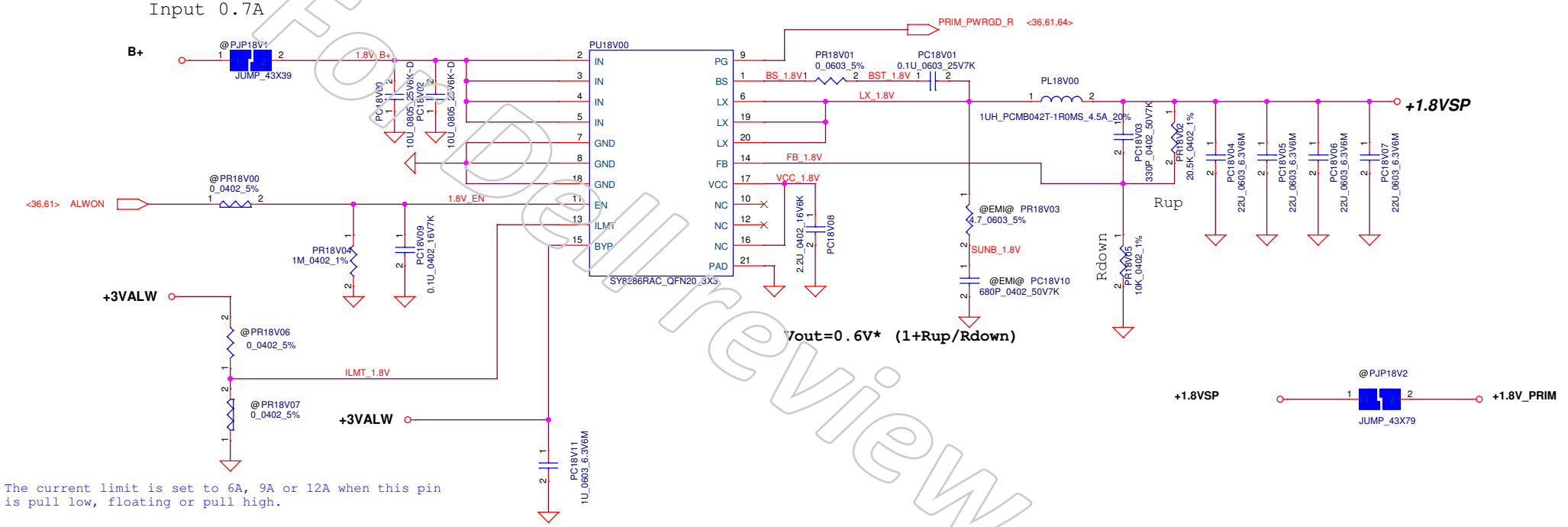
Input Current:0.227A

1.8*1.289/0.85/12V=0.227A

+1.8VSP
TDC 1.289A
Peak Current 1.842A
OCP current 6A
FSW=500KHz
TYP MAX
DCR: 24mohm 27mohm

Input 0.7A



The current limit is set to 6A, 9A or 12A when this pin is pull low, floating or pull high.

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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Title: **PWR_+1.8VSP**

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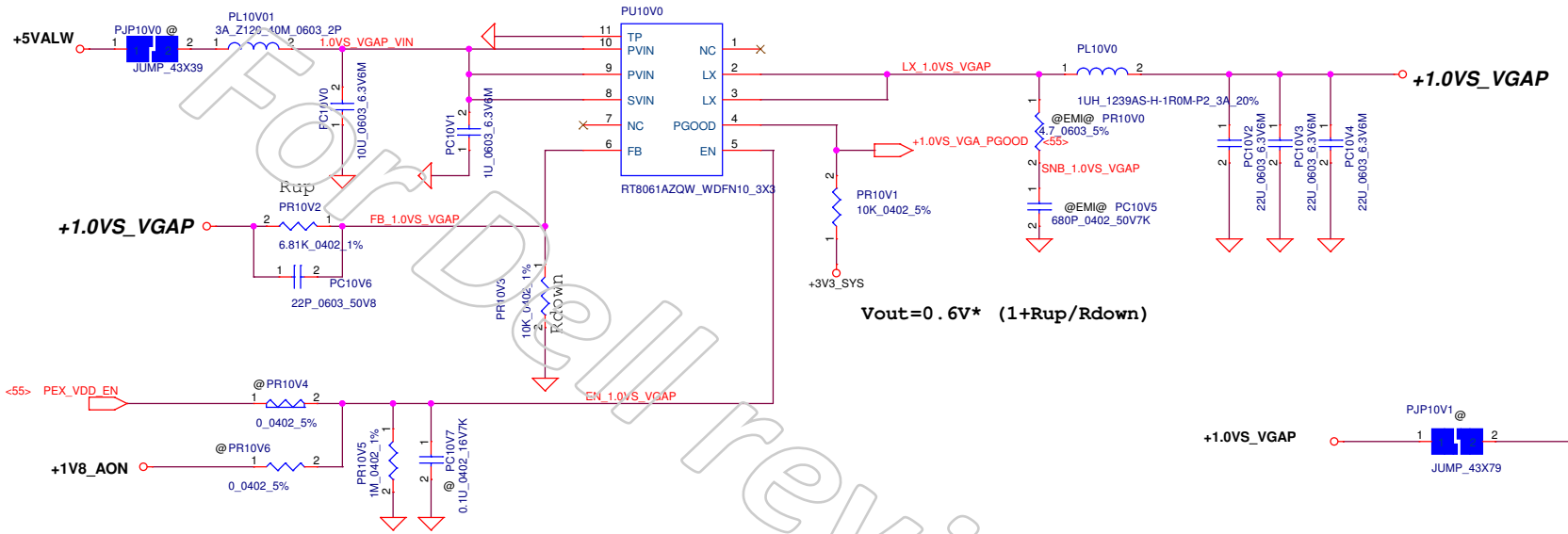
Input Current:0.231A

1*0.9835/0.85/5=0.231A

+1.0VS_VGAP
TDC 0.9835A
Peak Current 1.405A
OCP current 4A
FSW=1MHz

	TYP	MAX
DCR	45mohm	59mohm



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: PWR_+1.0VS_VGA

Size | Document Number: LA-E992P | Rev: 0.3(X02)

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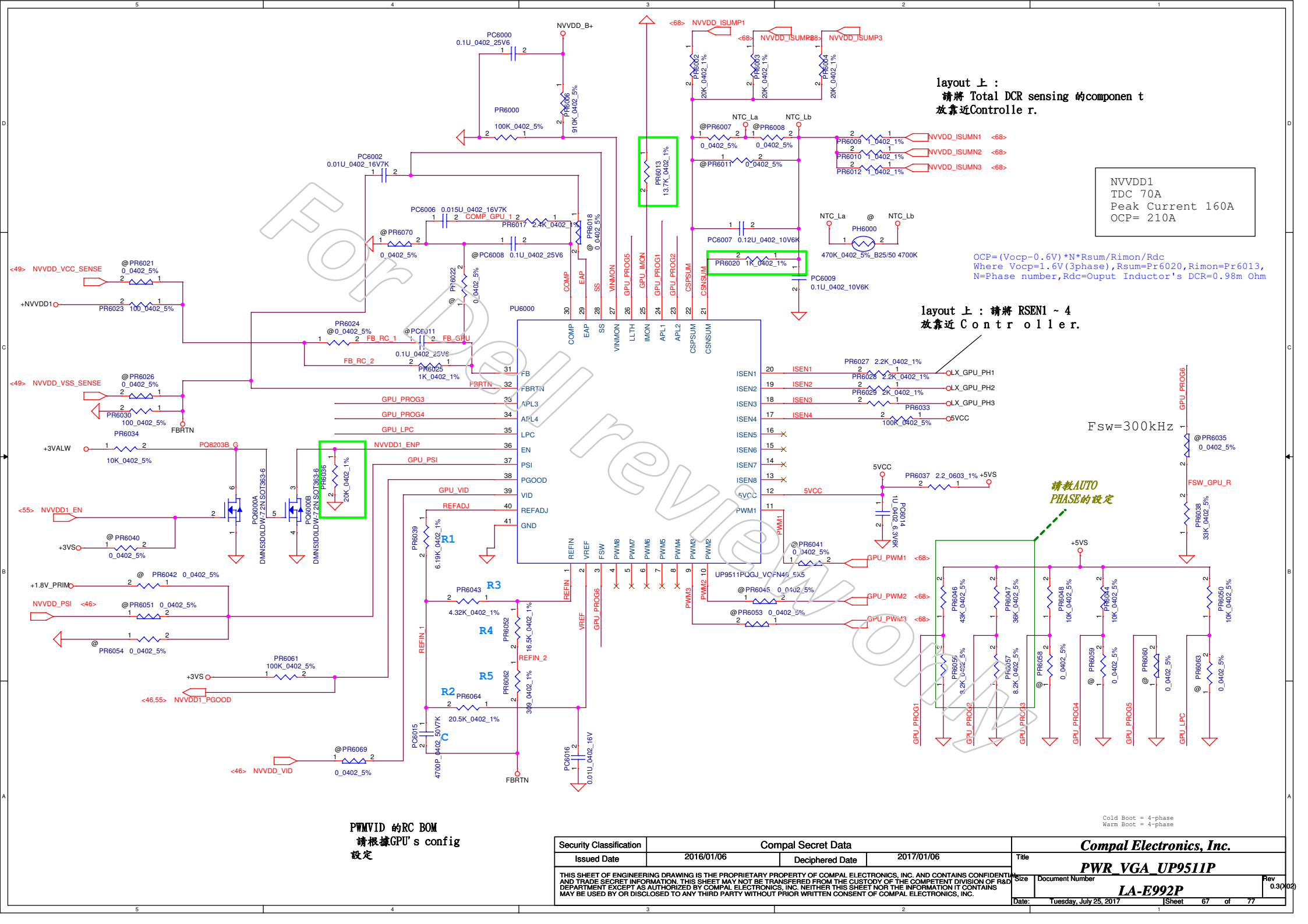

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.			
Title	PWR_VGA_UP9511P		
Size	Document Number		Rev
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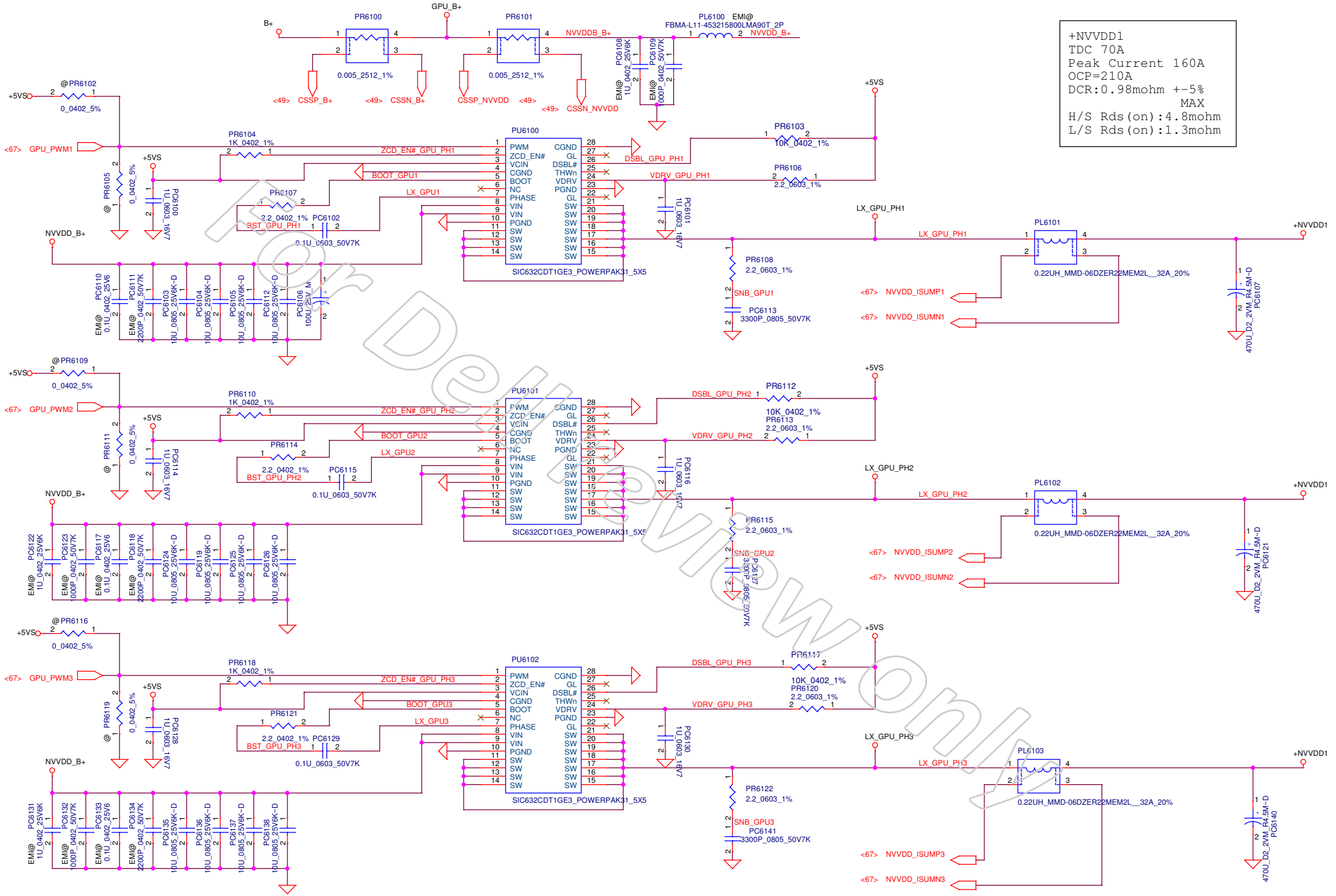

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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Title: **PWR_+NVVDD1**

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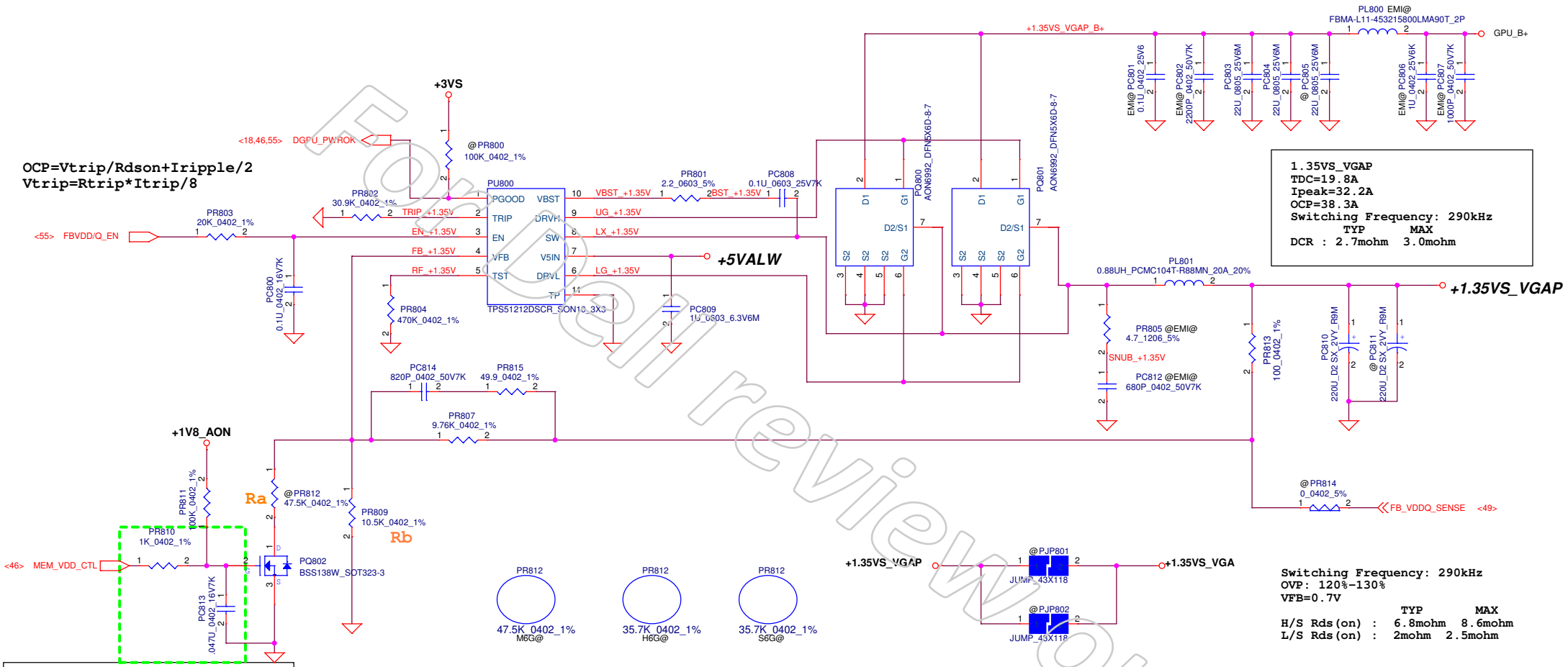
Input Current: 2.074A
1.35V*15.67A/0.85/12V=2.074A



N17E-G2/-G1 MAX-Q:
P0:4004MHz,FBVDD=1.55V/1.50V
P2:3802MHz,FBVDD=1.55V/1.50V
P3:3003MHz,FBVDD=1.35V
P5:810MHz,FBVDD=1.35V
Idle(P8):405MHz,FBVDD=1.35V

If MEM_VDD_CTL high:
Ra=47.5Kohm,Rb=10.5Kohm
Ra//Rb = 8.599kohm
Vout=0.704*(1+(9.76/8.599))=1.503V

If MEM_VDD_CTL low:
Vout=0.704*(1+(9.76/10.5))=1.358V

If MEM_VDD_CTL high:
Ra=35.7Kohm,Rb=10.5Kohm
Ra//Rb = 8.114kohm
Vout=0.704*(1+(9.76/8.114))=1.5508V

If MEM_VDD_CTL low:
Vout=0.704*(1+(9.76/10.5))=1.358V

BOM config	GPU type	VRAM memory	VRAM vender	RVL	PR809	PR812	PR807
X7673331L07	N17E-G1 MAXQ	256Mx32	Samsung	1.35V & 1.55V	10.5K	35.7K	9.76K
X7673331L08	N17E-G1 MAXQ	256Mx32	Hynix	1.35V & 1.55V	10.5K	35.7K	9.76K
X7673331L09	N17E-G1 MAXQ	256Mx32	Micron	1.35V & 1.5V	10.5K	47.5K	9.76K

Security Classification	Compal Secret Data		
Issued Date	2014/2/11	Deciphered Date	2014/2/11

Compal Electronics, Inc.

Title: **PWR-1.35VRAM**

Size | Document Number: **LA-E992P** | Rev: 0.3(X02)

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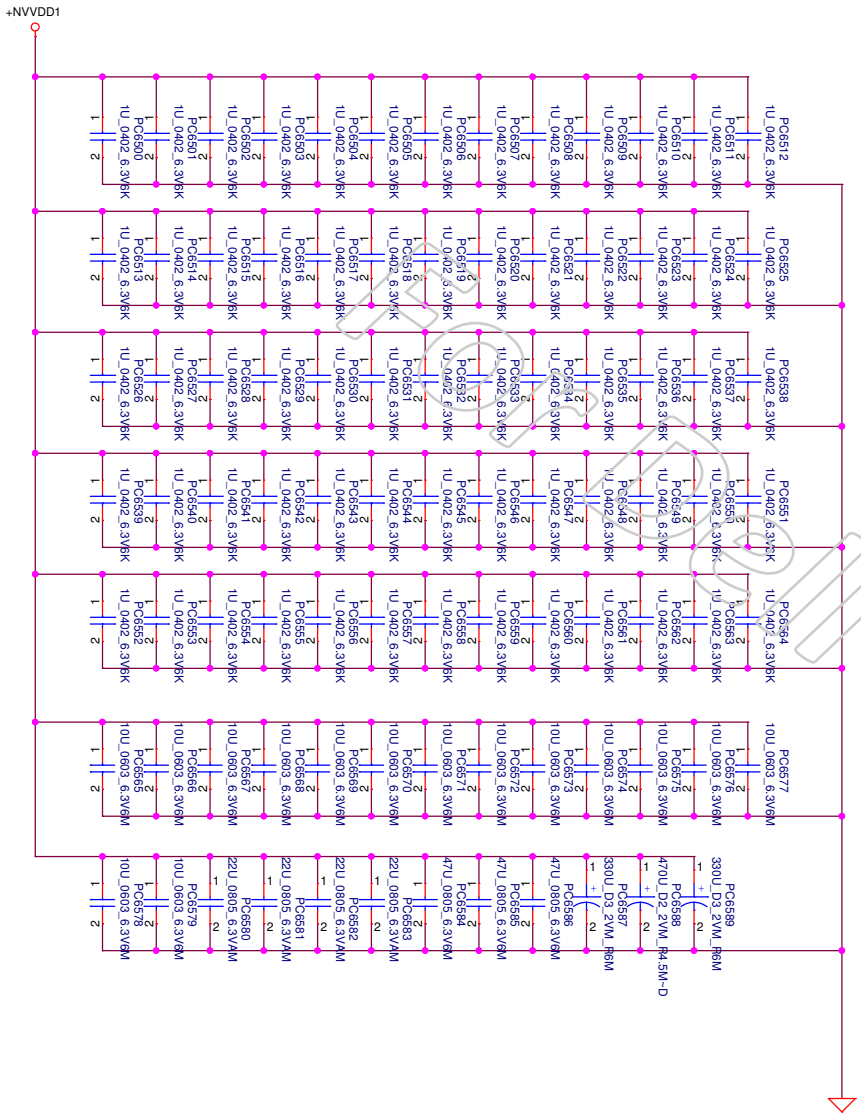


```
+NVVDD
470uF X 1
330uF X 2
47uF_0805 X 3
22uF_0805 X 4
10uF_0603X 15
1uF_0402 X 65
```


Security Classification	Compal Secret Data		
Issued Date	2015/09/18	Deciphered Date	2016/09/18

Compal Electronics, Inc.

Title: **VGA DECOUPLING**

Size | Document Number: **LA-E992P** | Rev: 0.3(X02)

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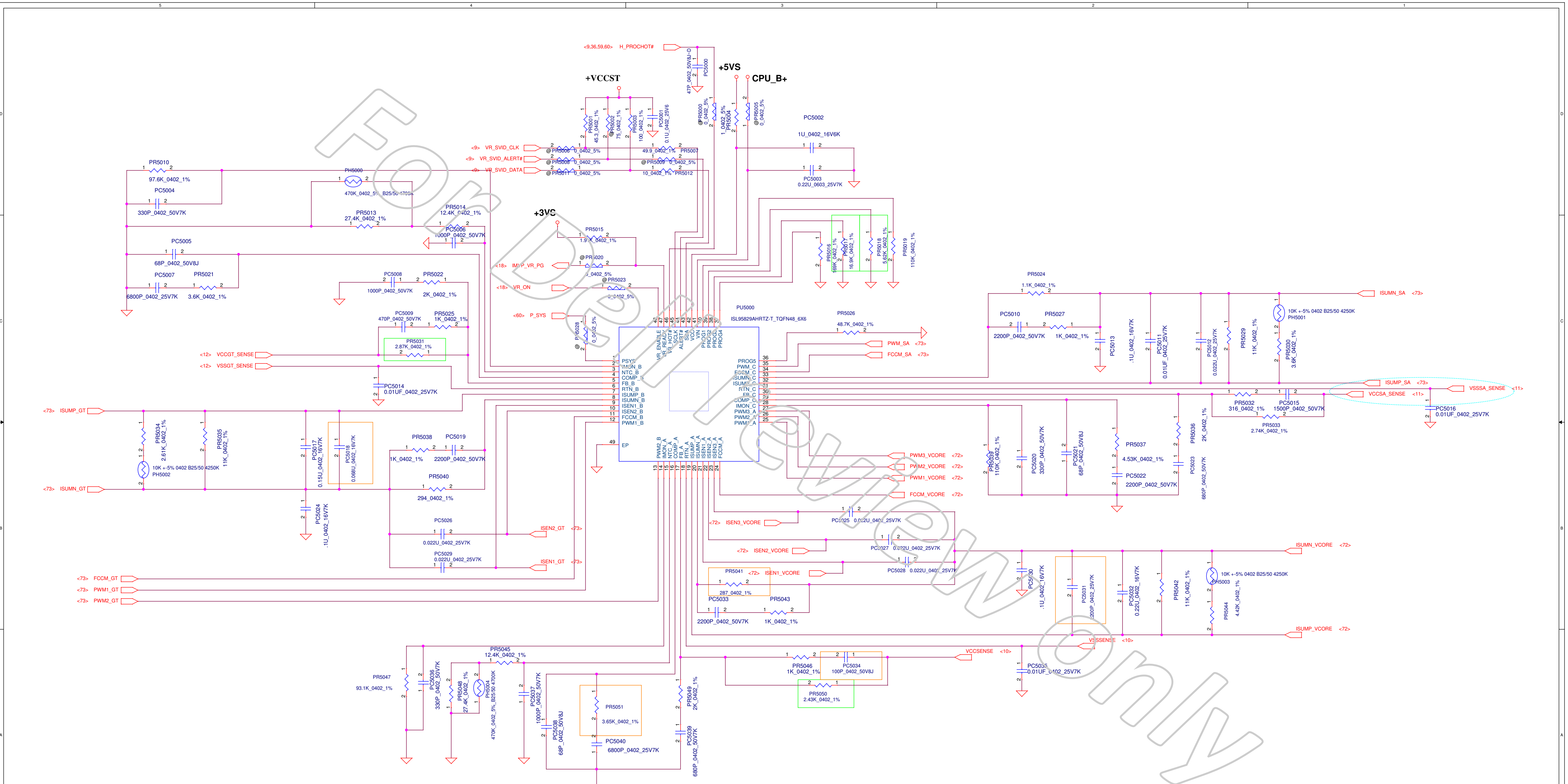


Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.

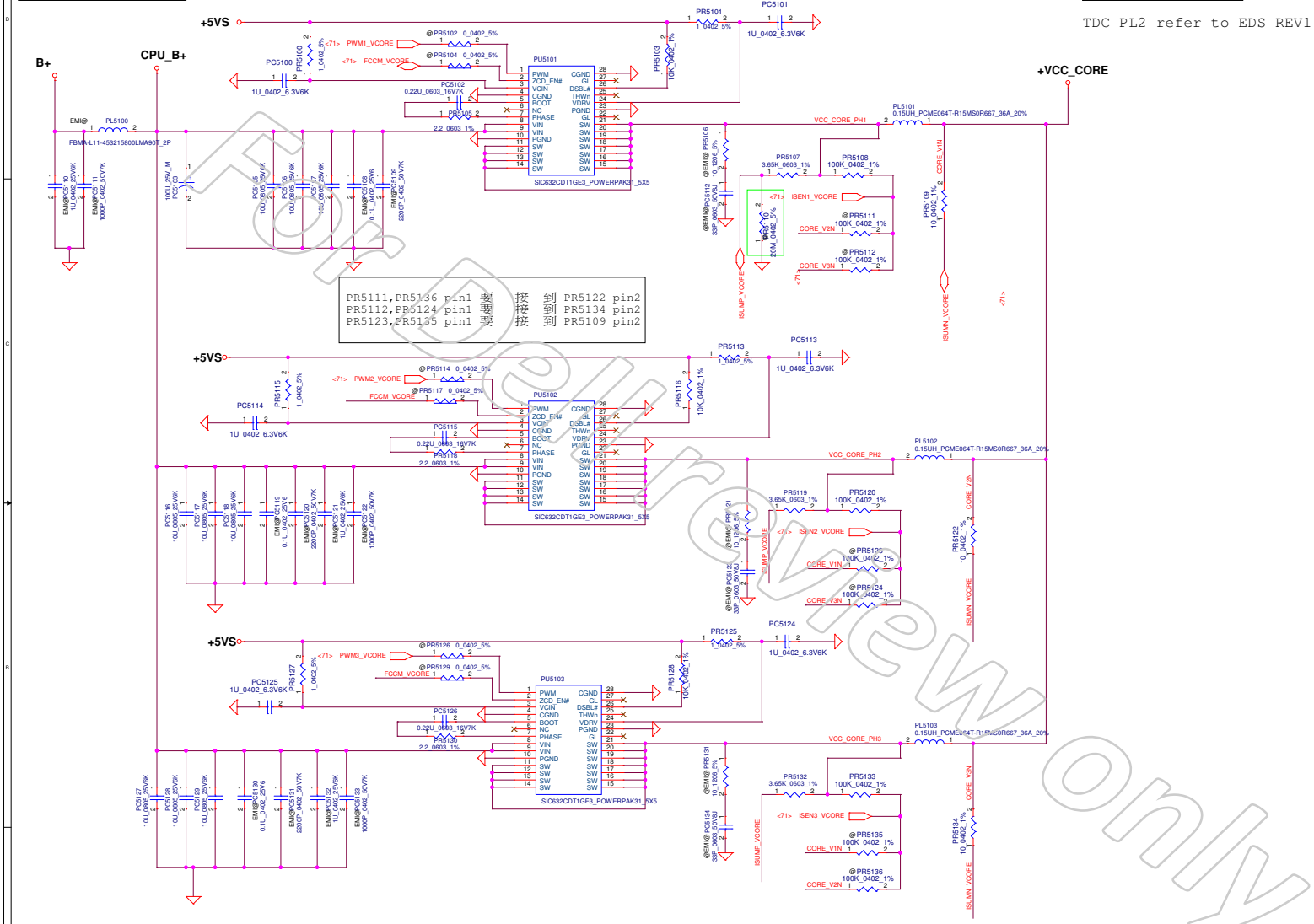
Title: PWR_VCORE_ISL95855

Size | Document Number: LA-E992P | Rev: 0.3(X02)

Input Current: 7A
1.5V*47.6A/0.85/12V=7

+VCC_CORE
TDC PL2 :50A
Peak Current 70A
OCP Current 82A
DCR 0.66mohm +/-7%
Load Line 1.8mV/A

TDC PL2 refer to EDS REV1.5



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/01/06	Deciphered Date	2017/01/06
Title	PWR_VCORE +VCC_CORE		
Size	Document Number		Rev
	LA-E992P		0.1(X02)
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Input Current: 5.66A
1.5V*38.5A/0.85/12V=5.66

+VCC_GT
TDC PL2 :25A
Peak Current 55A
OCP Current 66A
DCR 0.66mohm +/-7%
Load Line 2.65mV/A

+5VS
CPU_B+
+VCCGT
PU5201
SIC632CDT1GE3_POWERPAK31_5X5
PR5211 pin1 要 接 到 PR5221 pin2
PR5222 pin1 要 接 到 PR5209 pin2

+VCC_SA
TDC PL2 :10A
Peak Current 11.1A
OCP Current 13.32A
DCR 6.2mohm +/-5%
Load Line 9.1mV/A

+5VS
CPU_B+
+VCCGT
PU5202
SIC632CDT1GE3_POWERPAK31_5X5

Input Current: 0.8A
1.05V*7.77A/0.85/12V=0.8

CPU_B+
+VCCSA
PU5203
SIC531CDT1GE3_POWERPAK22_4X3
+5VS

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: PWR_VCORE_+VCCGT,+VCCSA

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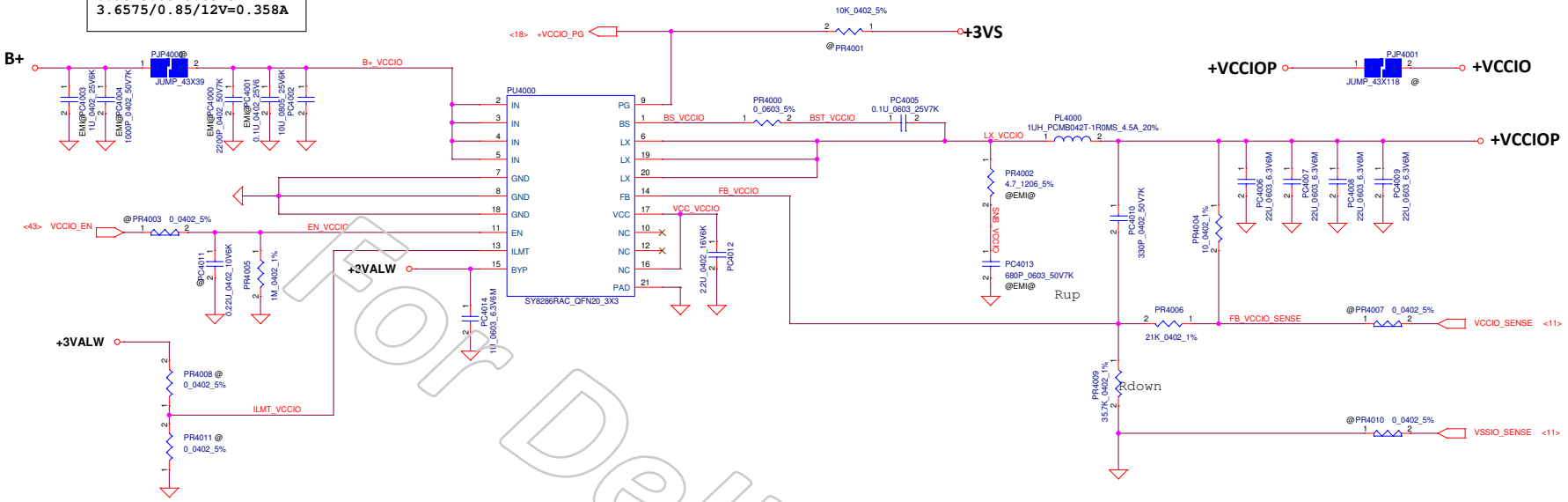
Input Current:0.358A

0.95*3.85=3.6575W
3.6575/0.85/12V=0.358A



The current limit is set to 6A, 9A or 12A when this pin is pull low, floating or pull high.

+VCCIOP (0.95V)
TDC 3.85 A
Peak Current 5.5 A
OCP Current 9 A Fix by IC
FSW:500KHz

	TYP	MAX
DCR	24.0mohm	27.0mohm

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: PWR_+VCCIO

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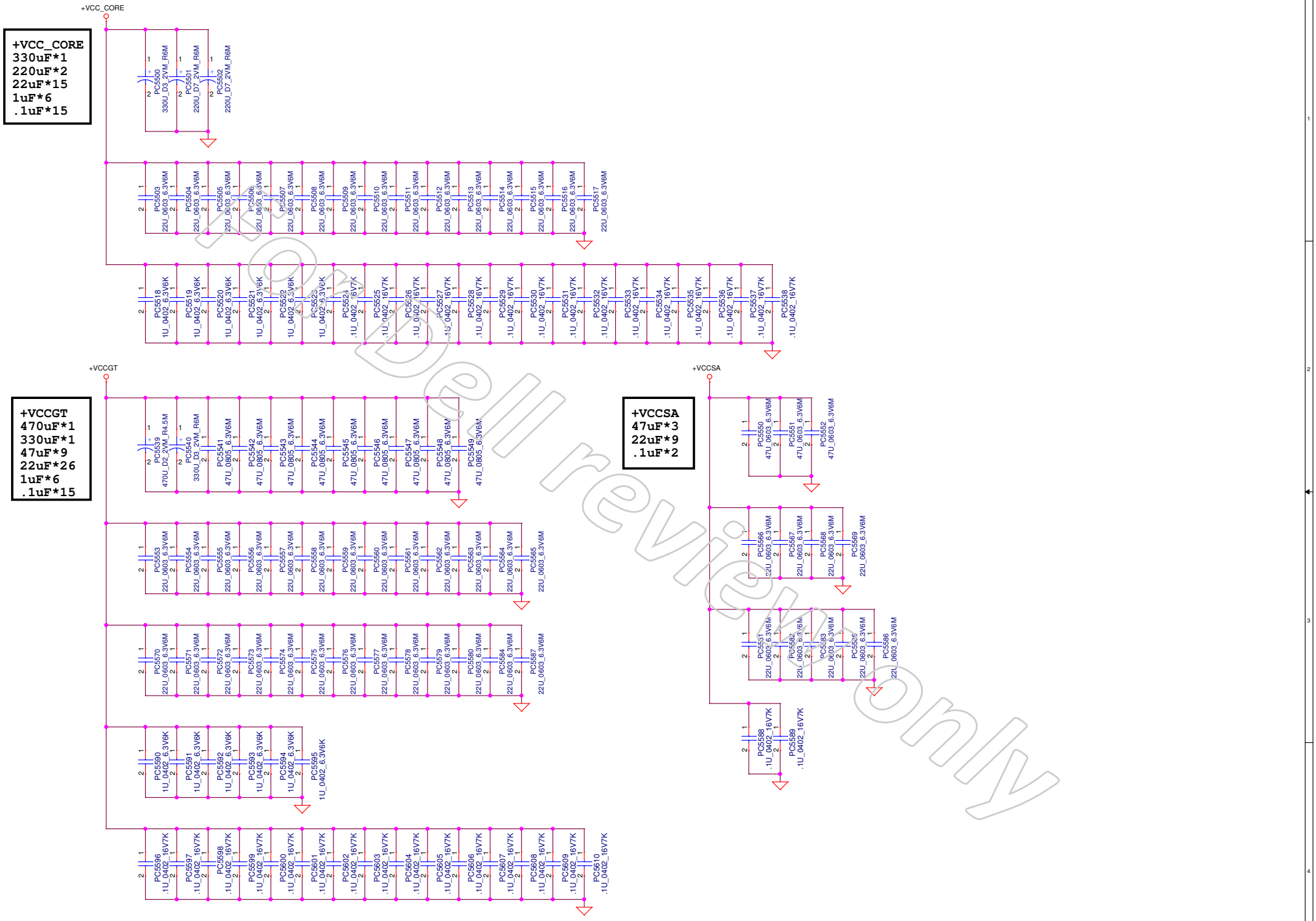

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.			
Title	PWR_CPU DECOUPLING		
Size	Document Number		Rev
B	LA-E992P		0.3(X02)
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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	60	CHARGER	2017/01/09	Compal_PWR	Modify ILMT.	1. Change PR714 from 20K(@) Ohm to 20K Ohm. 2. Change PR715 from 1.17K(@) Ohm to 5.76K Ohm	0.1
2	69	+1.35VRAM	2017/01/09	Compal_PWR	For BOM control	1. Add PR812 of 35.7k Ohm for S6G@ 2. Add PR812 of 35.7k Ohm for H6G@ 3. Add PR812 of 47.5k Ohm for M6G@	0.1
3	65	+1.8VGSP	2017/01/09	Compal_PWR	For EE request to add capacitor for avoiding noise	1. Change PC18V09 form 0.1u(@)F to 0.1uF.	0.1
4	61,64	+3/+5VALWP & +1VALWP	2017/02/13	Compal_PWR	Avoid to use Samsung Capcitor in common part, change to independent P/N.	1. Change PC103,PC104,PC301,PC302,PC307,PC308 from SE00000QK00 to SE00000QK0L	0.1
5	67	VGA_UP9511	2017/02/17	Compal_PWR	Avoid 5VCC leakage issue, so we amplify the divider resistance	1. Change PR6000 form 10K Ohm to 100K Ohm 2. Change PR6006 from 91K Ohm to 910K Ohm	0.1
6	59	DCIN / BATT CONN /OTP	2017/02/22	Compal_PWR	Follow EE's request,use the same part with EE.	1. Change PQ6 from SB00000DH00 to SB00000ZU00 2. Change PQ7 from SB00000I700 to SB00000ZU00	0.1
7	59,60	DCIN / BATT CONN /OTP & Charger	2017/03/02	Compal_PWR	Follow Dell &EC request,change I_ADP 's net name.	1. Change net name from I_ADP to I_ADP_R	0.1
8	60	Charger	2017/03/03	Compal_PWR	Before EC program AC_DIS is floating. Avoid the siganal forcing PQ708 open quickly, add pull down resistor on AC_DIS siganal.	1. add PR734 100K Ohm on siganal AC_DIS	0.1
9	66	+1.0VS_VGA	2017/03/03	Compal_PWR	Follow EE's request,change enable siganl.	1. Change net name from NVVDD1_EN to PEX_VDD_EN.	0.1
10	60	Charger	2017/03/06	Compal_PWR	Follow sourcer request,change PD part.	1. Change PD700 from SCS00005400 to SCS00003800.	0.1
11	69	+1.35VRAM	2017/03/07	Compal_PWR	The VRAM voltage will switch between 1.5V and 1.35V, there will be a overshoot voltage.To solve this issue, we add 1K ohm and 47nF.	1. Change PR810 from 0 ohm to 1K ohm 2. add 47nF PC813 from PQ802 gate to source.	0.1
12	65	+1.8VGSP	2017/03/14	Compal_PWR	Follow EE's request,modify output voltage to solve 1.8VS drop test.	1. Change PR18V02 from 20K ohm to 20.5K ohm	0.1
13	61	+3/+5VALWP	2017/03/14	Compal_PWR	Follow EE's request,modify output voltage to solve TypeC VBUS drop test.	1. Change PR301 from 15K ohm to 15.4K ohm	0.1
14	69	+1.35VRAM	2017/03/14	Compal_PWR	The VRAM voltage will switch between 1.5V and 1.35V, there will be a overshoot voltage.To solve this issue, we add 49.9 ohm and 1.5nF.	1. add PC814 and PR815 parallel with PR807.	0.1
15	69	+1.35VRAM	2017/03/14	Compal_PWR	Avoid the mos PQ802 won't open,so we change the lower Vth 's Mos (Vth=1.5V)	1.Change PQ802 from SB00000ST00 to SB00000T000.	0.1
16	59	DCIN / BATT CONN /OTP	2017/03/16	Compal_PWR	Dell request us to change PD1 's position.	1.Change PD1's Pin2 from PSID-0 to PSID.	0.1
17	71	VCORE-ISL95829	2017/03/20	Compal_PWR	After CPU VRTT Test,we tune some resistor&capcitor.	1. Change PR5041 from 267 ohm to 287 ohm. 2. Change PC5031 from 4700 pF to 2200 pF. 3. Change PR5051 from 4.87K ohm to 3.65K ohm. 4. Change PC5034 from 470 pF to 100 pF. 5. Change PC5018 from 33 nF to 68 pF.	0.1
18	69	+1.35VRAM	2017/03/23	Compal_PWR	Because FBVDDQ transient noise issue,so we follow EE's request,remove 220uF*1 output cap.	1. Change PC811 220uF to 220uF(@)	0.1

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/02	Deciphered Date 2013/10/28	Title NOTE

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	73	VCORE_+VCCGT_+VCCSA	2017/05/05	Compal_PWR	Because VCCSA's Choke DCR value would impact VRTT test result, so we choose SH000015M00 and SH000015P00 with same DCR value as main and 2nd source.	1. Change PL5203 from SH00000T500 to SH000015M00.	0.2
2	61	+3VALWP	2017/05/08	Compal_PWR	Modify +3VALWP OCP resistor.	1. Change PR304 from 8.87K ohm to 6.19K ohm.	0.2
3	69	+1.35VRAM	2017/05/08	Compal_PWR	Modify +1.35VRAM OCP resistor.	1. Change PR802 from 30.9K ohm to 42.2K ohm.	0.2
4	71	VCORE_ISL95829	2017/05/08	Compal_PWR	Modify VCCSA IMON resistor.	1. Change PR5024 from 1.27K ohm to 1.1K ohm.	0.2
5	59	DCIN	2017/05/08	Compal_PWR	Because DC-IN Cable is hard to plug and pull,we change dc-in beed from 2 pcs to 3 pcs.	1. Change PL1/PL2 from SM010008E10 to SM01000C000. 2. Add PL6=SM01000C000.	0.2
6	59	DCIN	2017/05/10	Compal_PWR	Adjust the battery unplug prochot delay time.	1. Change PC12 from 1uF to 0.1uF.	0.2
7	59	DCIN / BATT CONN / OTP	2017/05/11	Compal_PWR	Add another circuit to pull down the GPU power level.	1. Add PC16 0.1uF 2. Add PQ9=SB00000ST00. 3. Add PR34 0 ohm. 4. Add PR35 100Kohm.	0.2
8	59~74	All page	2017/06/22	Compal_PWR	For schematic cost down	1.Change PR721,PR706,PR723,PR730,PR733,PR6069,PR315,PR6051, PR6070,PR6035,PR5028,PR814,PR5011,PR6021,PR6018,PR101,PR103, PR5129,PR5213,PR705,PR732,PR5117,PR6026,PR5006,PR5102,PR731, PR5023,PR6060,PR727,PR6041,PR6045,PR5202,PR5215,PR4007,PR5020, PR5114,PR4003,PR5000,PR5005,PR5008,PR5224,PR5204,PR312,PR4010, PR5223,PR5009,PR5104,PR10V4,PR24,PR18V00,PR209,PR311,PR25,PR5126, PR211,PR25V00,PR18V07,PR6053,PR34 from 0 ohm to shortpad.	1.0
9	69	+1.35VRAM	2017/06/22	Compal_PWR	The VRAM voltage will switch between 1.5V and 1.35V, there will be a overshoot voltage.To solve this issue. we add 49.9 ohm and 820pF.	1. add PC814 and PR815 parallel with PR807.	1.0
10	69	+1.35VRAM	2017/07/11	Compal_PWR	Modify OCP resistor.	1.Change from 42.2Kohm to 30.9Kohm.	1.0
11	61	+5VALWP	2017/07/11	Compal_PWR	Modify OCP resistor.	1.Change from 16.5Kohm to 10.5Kohm.	1.0
12				Compal_PWR			
13				Compal_PWR			
14				Compal_PWR			
15				Compal_PWR			
16				Compal_PWR			
17				Compal_PWR			

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Issued Date	2011/06/02	Deciphered Date 2013/10/28	Title NOTE
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